The Early Days of GaAs ICs

Rory L. Van Tuyl, *Fellow, IEEE*

***Abstract*—This article recounts the author's experiences in the period 1972 – 1982, when GaAs ICs were new, technology was still developing, and each new result was the first of its kind.**

***Index Terms*—Gallium Arsenide, High-Speed Integrated Circuits, Integrated Circuit Fabrication, History.**

I. Introduction

TIMING is everything. By the 1970s the world was ready for GaAs ICs, and I was privileged to play a part in bringing them into existence. It had all started a century before when, in 1871, Dmitri Mendeleev predicted there should be a metallic element to fill the vacant position #31 in his *Periodic Table of the Elements*. In 1874 Frenchman Paul Émile LeCoq identified this element via spectroscopic analysis of zincblende ore, and named it Gallium. But Gallium does not occur in elemental form in nature, so it had to be laboriously extracted and thus was still a rare substance in 1927 when geochemist V. M. Goldschmidt first combined it with Arsenic. As III-V compound pioneer Heinrich Welker put it:

> "No one saw any technical application for these [III-V] compounds…They thus remained a laboratory curiosity." [1]

Until the invention of the transistor, that is. If column IV elements such as Germanium were useful semiconductors, why not chemical combinations of column III and V elements, which were by then known to have crystal structures similar to Germanium? So in 1951 Welker undertook research to answer the basic question: "Are III-V compounds semiconductors?" By the following year, having grown and characterized an ingot of semiconducting polycrystalline InSb, he had proved the point [2]. By 1955, single-crystal GaAs had been grown and used to build photocells [3, 4].

Just four years later, in July 1959, Robert Noyce filed for a patent (based on the Fairchild planar silicon bipolar transistor process) that for the first time described the monolithic silicon integrated circuit [5]. Lacking a suitable 3-terminal electronic device, GaAs was ineligible for the subsequent IC explosion of the early 1960s, but materials work intensified as researchers developed semi-insulating GaAs substrates and methods for growing doped epitaxial layers [6-9]. The GaAs device breakthrough came in 1965 when Carver Mead, using material supplied by Texas Instruments, fabricated and tested the first GaAs field-effect transistor with Schottky-barrier gate [MESFET] [10]. Subsequently, researchers in the U. S. and Europe improved the GaAs MESFET's performance until, by the early 1970s when it became possible to fabricate devices with 1μm gate lengths, GaAs MESFETs emerged as the first 3-terminal device capable of useful microwave amplification [11-14].

By 1972, all the elements were in place. GaAs ICs were waiting to be born.

II. The Research Phase

A. The First Circuits

In mid-1972, while working as an IC and RF/Microwave design engineer at Hewlett Packard's Santa Clara Division, I contacted Charles Liechti at the Company's central research facility, HP Labs. Charles had recently reported HP's first GaAs MESFET [14], and I was interested to see how this device might perform as a high-speed switch. (These MESFETs boasted f_T=15 GHz, versus 2 GHz for Si bipolar transistors of the time). Of the two chips I obtained for packaging, only one survived, but it functioned quite well. Switching speed was about 60ps, and I observed no anomalous switching effects. (As I would later discover, this device was exceptional: most MESFETs of the time were afflicted with switching anomalies. Had this first device I measured been "typical", my career and GaAs ICs might have taken separate paths). HP Labs wanted to compete for an Air Force contract to build digital ICs in GaAs. No one had yet done this, and HPL at the time was well-equipped to take on the challenge. In 1966, as they entered the Light-emitting Diode business, HP had learned the secrets of how to grow GaAs with the Horizontal Bridgman technique, and how to deposit epitaxial layers of GaAsP using Liquid Phase Epi [LPE]. It was this technology that had been used for the 1972 MESFET work at HP Labs. What HPL now needed was someone experienced in high-frequency IC design and test, someone who could help them obtain and execute a program they hoped the Air Force would fund. In the fall of 1972 I co-authored a proposal for this Air Force contract, and by year's end – little suspecting what obstacles lay ahead - had transferred to HP Labs to begin the great adventure.

Work began even before we received the contract in March, 1973 [15]. With more devices now available to test, I was dismayed to discover that every sample was crippled by what I soon dubbed *lag effect*. They would switch OFF completely in picoseconds, but when switching ON from the fully OFF state, complete switching took tens of microseconds!

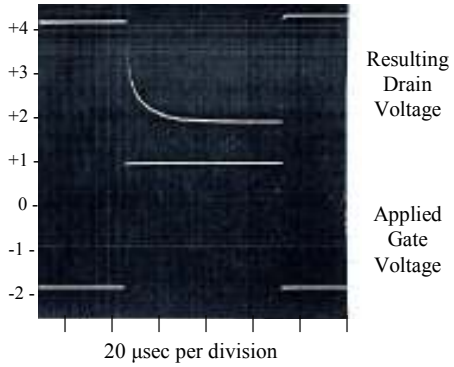

Fig. 1. On October 30, 1972, after joining HP Labs, I first discovered the *Lag Effect*. Since only 25% of the drain current responded immediately to a change in gate voltage, this rendered MESFETs useless as switches.

After months of thought and experimentation, we decided that *lag effect* must be caused by surface state depletion in the regions adjacent to the metallic gate. With extra care we could minimize it, but to eliminate it we would need to change the process to reliably ensure a tighter fit between the gate and its etched channel. Initial attempts at a self-aligned gate process failed [16], but subsequent process changes (finally implemented in 1974) succeeded in killing *lag effect.*

In December, 1972 I designed what was to become the world's first GaAs MESFET integrated circuit [17]. It was a crude affair, a simple NAND/NOR gate with active load and a separate buffer/level-shifter that needed to be wire bonded to the logic gate.

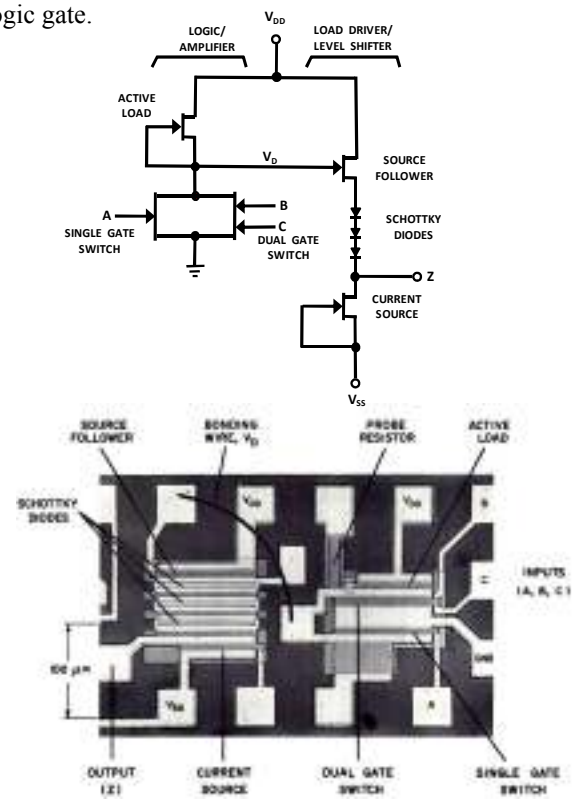

Fig. 2. The world's first GaAs MESFET logic gate, 1973.

When finally tested in September, 1973, this logic circuit performed well, exhibiting record propagation delay for the time [18-20].

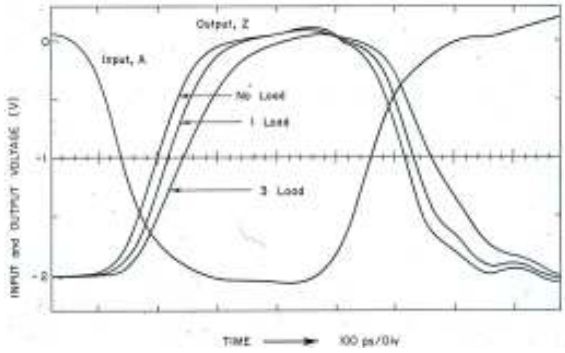

Fig. 3. The NAND/NOR logic gate showed 60ps delay with one output load, 75ps with two loads, 105ps with three loads.

B. Medium-Scale Integrated Circuits

In early 1974, we undertook to build medium-scale GaAs ICs [MSI] with useful performance and complexity. This would require several key improvements:

Improved material. LPE n-type epi layers were non-uniform, so poor MSI yields could be expected with LPE. We experimented with alternatives: vapor-phase epi [VPE]; diffused n-layers; and ion implantation into LPE buffer layers. We settled on ion implantation.

Layout miniaturization. This required two levels of metal, which we isolated with a barely-adequate layer of evaporated SiO. We made do with the existing device isolation process: mesa etching. A serious problem arose with miniaturization: *sidegating.* Imperfect dc isolation between devices caused reduction of current in devices operating at voltages above the most negative in the circuit.

Computer-aided design. I had developed the first non-linear computer model of the MESFET in 1974 [16]. It became a useful tool by 1975, despite the fact that simulations had to be run on the HP corporate IBM mainframe, and were impossible to obtain at month's end when payroll was being processed!

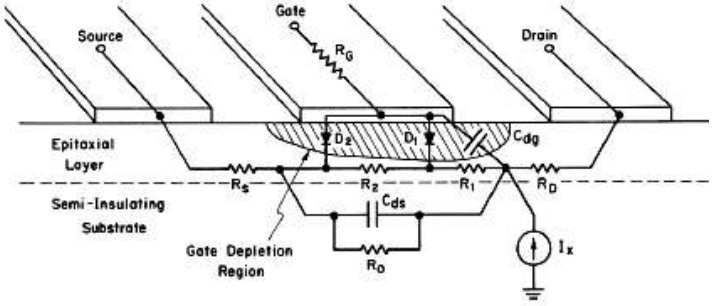

Fig. 4. The 1974 non-linear MESFET device model was based on a 2-lump approximation of the FET channel. Pinchoff was proportional to square root of gate voltage, but velocity saturation - approximated by the hyperbolic tangent function – mimicked the short-channel properties of the MESFET. This model became a key tool for subsequent IC design [21].

We reported circuits with these improvements in 1976 [22]. By May of that year, we were able to test optimized circuit designs fabricated on Se-implanted layers. The results, published in 1977 [23-25], are summarized here:

1. A static frequency divider with 4 GHz clock rate,
2. A gated divide-by-eight circuit with 2 GHz clock,
3. An 8:1 multiplexer operating to 3 Gb/sec.

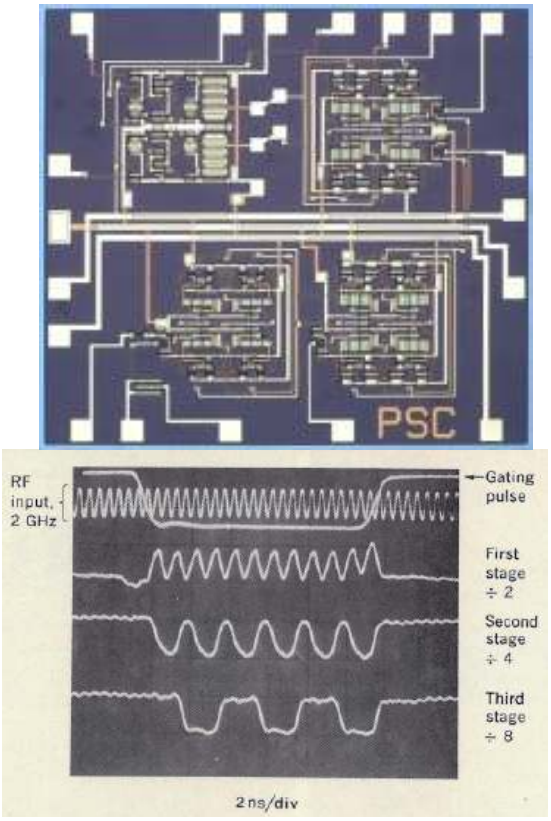

Fig. 5. Divide-by-eight gated prescaler with 2 GHz clock fabricated and tested at HP Labs in 1976.

C. *RFICs*

Even before conclusion of the previously-described work, I had developed a view of GaAs ICs that saw a more promising future for them in RF and microwave applications, with digital circuits limited to high-speed data applications and as adjuncts to RF circuitry [e.g. prescalers]. Silicon had by that time completely eclipsed GaAs in larger-scale applications. The factor-of-two or three speed advantage of GaAs over Si mattered most in the frequency domain, where a doubling of bandwidth was a crucial contribution. In 1976, I bootlegged some experimental dc-4GHz amplifiers on the digital mask set, and initial test results looked promising [26]. In 1977 I transferred to HP's Santa Rosa Division where, working with Derry Hornbuckle, we expanded the direct-coupled amplifier work to multiple stages and higher output powers [27].

The *pièce de résistance* of this period was a multifunction RFIC, the first of its kind in GaAs, incorporating a tunable local oscillator with amplitude adjustment, balanced mixer, ON/OFF modulator and I. F. amplifier on a single chip [28-29].

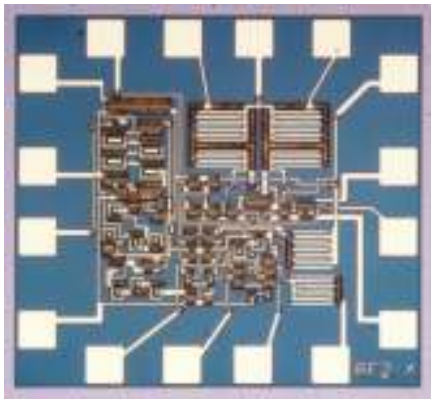

Fig. 6. The RF Signal Generation chip of 1978/79. The local oscillator tuned 2.1-2.5 GHz using on-chip tuning diodes and an off-chip inductor. The downconverted I.F. was dc – 1.4 GHz.

IV. THE PRODUCTION DEVELOPMENT PHASE

All HP GaAs ICs through 1978 had been processed either at HP Labs or at HP's Santa Rosa Technology Center [SRTC] using essentially the process we had developed at HPL under the digital IC contract. This process was far from production-worthy, so in 1979 the decision was made to staff up a project to develop a production process. I was transferred to SRTC to head this project. We needed to have MESFETs with repeatable characteristics, a planar process free from the curse of mesa isolation, and a reliable dual-level metal system with defect-free intermetal dielectric. We were fortunate to be supported by an existing process infrastructure originally built for discrete Si transistors and now running production GaAs FETs. Ion implantation was in place and we were lucky enough to have a project in-house for growing semi-insulating GaAs by the liquid-encapsulated Czochralski [LEC] process. Key developments over the period 1978 – 1981 included [30-31]:

- Semi-insulating GaAs free from Cr doping (LEC could be grown with a natural deep-level acceptor called EL2);
- At long last: *Round Wafers*!
- Silicon ion implantation directly into bulk material, obviating the need for an epitaxial buffer layer;
- Low pressure chemical-vapor-deposited [LPCVD] implant anneal cap that remained in place as a field oxide for metal lift assist;
- Proton isolation of conductive areas to replace mesa isolation, reduce sidegating and ensure planarity;
- Silicon nitride deposited by plasma-enhanced CVD to passivate the MESFETs and double as a dielectric film for capacitors;
- Reliable metallization [Mo-Au and Cr-Pt-Au] to replace the Cr-Au used in the research phase;
- Spun-on polyimide intermetal dielectric to support, isolate and overcoat the second metal;
- In-process control of MESFET Idss to within 10%;
- Semi-automated post-process testing with high-frequency wafer probes.

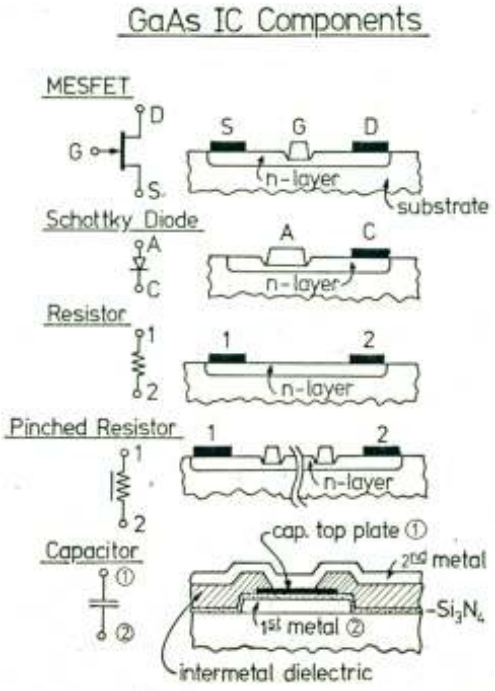

Fig. 7. The 1981 *RFIC Process* offered designers a complete set of components: MESFETs, Schottky Diodes, resistors and thin-film capacitors.

Fig. 8. The process featured passivated devices and fully-planar geometry made possible by proton isolation and polyimide intermetal dielectric.

V. CONCLUSION

During the decade 1972 – 1982, Hewlett Packard Company progressed from laboratory samples of discrete microwave MESFETs built with materials technology developed originally for LEDs, to a practical manufacturing process for RF and high-speed digital integrated circuits. Along the way, we demonstrated benchmark performance of digital and RF integrated circuits built with the ever-evolving process. By 1990, 24 custom-designed GaAs integrated circuits had shipped in HP test instruments: frequency counters, spectrum analyzers, signal generators, active probes, arbitrary waveform generators, pulse generators and digitizing oscilloscopes. From this beginning, HP – now Agilent Technologies – has continuously improved its III-V custom IC technology to include p-HEMT MMICs and HBT analog/digital circuits in both GaAs and InP systems.

REFERENCES

[1] H. Welker, “Discovery and Development of III-V compounds," in *IEEE Transactions on Electron Devices*, ED-23 (1976), 664-674.

[2] H. Welker, "Über neue halbleitende Verbendungen," in *Zeitschrift fur Naturgortschung 7A*, (1952) pp. 744-749.

[3] R. Gremmelmaier, “GaAs-Photoelement,” *Z. Naturforsch*, vol.10a, p. 501, 1955.

[4] R. Gremmelmaier, “Herstellung von InAs und GaAs-Einkristallen,” in Z. Naturforsch., vol. 11a, p. 511, 1956.

[5] “Semiconductor Device-and-Lead Structure,” United States Patent 2,981,887. Granted April 25, 1961.

[6] Welker [1976], pg. 670, notes that by 1964 over 1000 publications about III-V semiconductors were extant.

[7] G. Cronin, G. and R. W. Haisty, "The preparation of semi-insulating Gallium Arsenide by chromium doping," in *J. Electrochemical Society*, vol. 111, no. 7, pp. 874-877, July 1964.

[8] D.H. Nelson, RCA Rev. vol. 24, pg. 603 (1963) describes liquid-phase epitaxial growth [LPE] of GaAs.

[9] D. Effer, “Epitaxial growth of doped and pure GaAs in an open flow system,” in *J. Electrochem. Soc*., vol. 112, pg. 1020, 1965 describes early vapor-phase epitaxy [VPE].

[10] C. A. Mead, “Schottky barrier gate field effect transistor,” in *Proc. IEEE Lett.*, Feb. 1966, pp. 307-308.

[11] W. Hooper, and W. Lehrer, "An Epitaxial GaAs Field-Effect Transistor," in *Proc. IEEE*, July 1967, pp. 1237-1238.

[12] K. Drangeid and R. Sommerhalder, "Dynamic performance of Schottky-barrier field-effect transistors," in IBM J. Res. Develop., vol. 14, no. 2, pp. 82-94, Mar. 1970.

[13] W. Baechtold et al., "X and Ku band GaAs MESFET," in *Electron. Lett.* Vol. 8, no. 2, pp. 35-37, 1972.

[14] C. Liechti, E. Gowen and J. Cohen, "GaAs Microwave Schottky-Gate Field-Effect Transistor," in *ISSCC Dig. Tech. Papers*, pp. 158-159, Feb. 1972.

[15] Air Force Avionics Lab contract F33615-73-C-1242.

[16] Technical Report AFAL-TR-74-40 (March 1974). *Lag effect* was completely eliminated, but the process proved unreliable.

[17] HP Lab Notebook 1567, pg. 17, December 22, 1972. Years later, Richard Eden of Rockwell International would christen this circuit “Buffered FET Logic” [BFL].

[18] R. Van Tuyl and C. Liechti, "High-speed integrated logic with GaAs MESFETs," in *ISSCC Dig. Tech Papers*, 1974, pp. 114-115.

[19] Technical Report AFAL-TR-74-40 (March 1974).

[20] R. Van Tuyl and C. Liechti, "High-speed integrated logic with GaAs MESFETs," in *IEEE J. Solid State Circuits*, 1974, pp. 269 - 276.

[21] R. Van Tuyl, D. Hornbuckle and D. Estreich, "Computer Modeling of Monolithic GaAs IC's," in *1980 IEEE Mic. Symp. Dig.*, pp. 393-394.

[22] R. Van Tuyl and C. Liechti, "High-speed GaAs MSI," in *ISSCC Dig. Tech Papers*, 1976, pp. 20-21. The ion implantation layers for these and subsequent ICs was provided by Charles Stolte of HP Labs.

[23] R. Van Tuyl and C. Liechti, "4-GHz Frequency division with GaAs MESFET ICs" in *ISSCC Dig. Tech Papers*, 1977, pp. 198-199.

[24] R. Van Tuyl, C. Liechti, C. Stolte, Technical Report AFAL TR-76-264, April 1977.

[25] R. Van Tuyl, C. Liechti, R. Lee, E. Gowen, "GaAs MESFET Logic with 4GHz Clock Rate," in *IEEE J. Solid State Circuits*, 1977, pp. 485 - 496.

[26] R. Van Tuyl, "A Monolithic Integrated 4-GHz Amplifier" in ISSCC Dig. Tech Papers, 1978, pp. 72-73.

[27] D. Hornbuckle and R. Van Tuyl, "Monolithic GaAs Direct-Coupled Amplifiers," in *IEEE Trans. Elec. Dev.*, Feb. 1981, pp. 175-182.

[28] R. Van Tuyl, "A Monolithic GaAs FET RF Signal Generation Chip," in *ISSCC Dig. Tech Papers*, 1980, pp. 118-119.

[29] R. Van Tuyl, "A Monolithic GaAs IC for Heterodyne Generation of RF Signals," in *IEEE Trans. Elec. Dev.*, Feb. 1981, pp. 166-170.

[30] R. Van Tuyl, D. D’Avanzo, V. Kumar, T. Taylor, D. Hornbuckle, R. Fisher and V. Peterson, Papers 21, 23, 24 in *Research Abstracts of the GaAs IC Symposum,* October, 1981.

[31] R. Van Tuyl et al., "A Manufacturing Process for Analog and Digital Gallium Arsenide Integrated Circuits," in *IEEE Transactions on Microwave Theory and Techniques*, July, 1982, pp. 935-942.