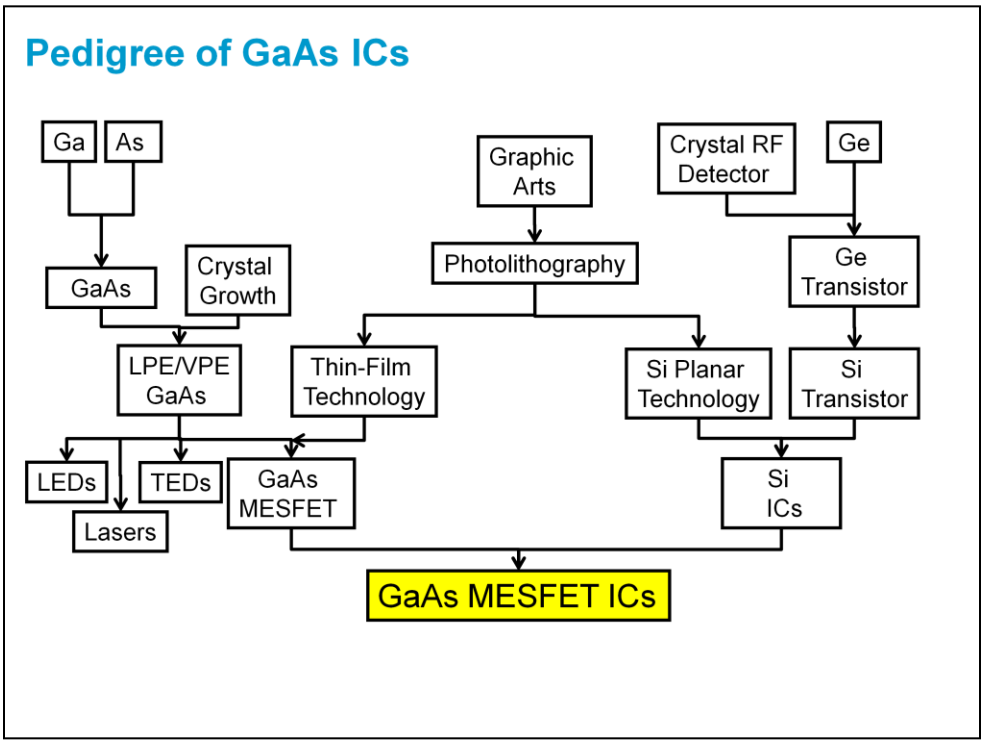
The Early Days of GaAs ICs

Recounting the author's experiences in the period 1972 – 1982, when GaAs ICs were new, technology was still developing, and each new result was the first of its kind.

Rory Van Tuyl
CSICS 2010
October 4, 2010

>Good morning. I'm really pleased to be here today at the 2010 Compound Semiconductor IC Symposium, and I'd like to thank Dan Scherrer and the program committee for the opportunity to speak here today.

- If any group should be interested in hearing about the early days of GaAs ICs, I guess it would have to be you
- There's a lot to cover, so let's get started…
- But first, let me say that this won't be a broad survey talk. After a bit of historical perspective, I'll be talking mostly about my own experiences in the decade 1972 through 1982, because that's what I know the most about and remember best.

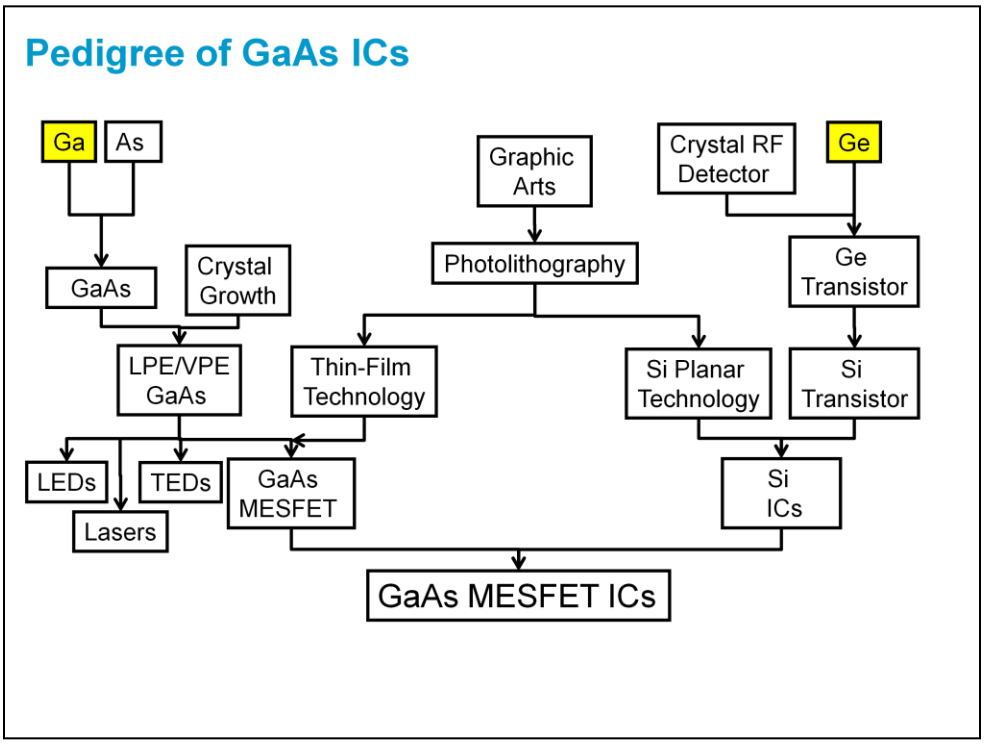


>Let's start with the Family Tree.

>There were a whole lot of precursor technologies that brought GaAs ICs into the world in the 1970s

>The "mother" and "father" technologies, so to speak, were the GaAs MESFET and the Silicon IC, both born in the 1960s

>And each of these technologies in turn has its own genealogy

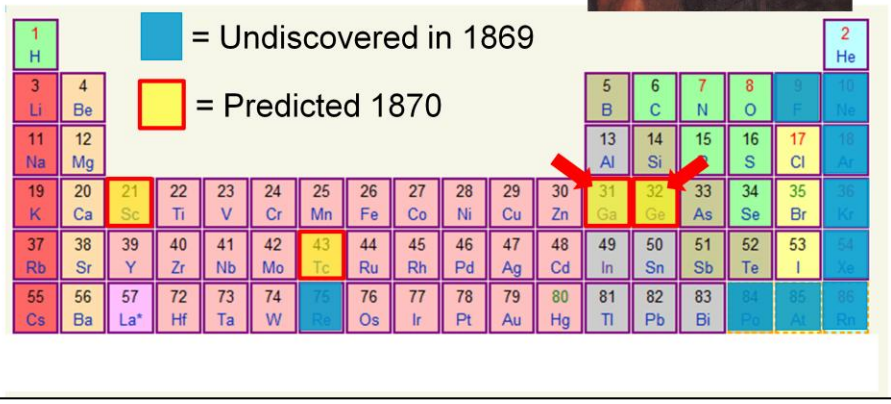


>Let's follow these two family branches back 100 years, right to the emergence of two basic materials, Gallium and Germanium

Mendeleev's Predicted Elements

The Periodic Table of 1869 had some gaps

The existence and properties of Gallium and Germanium were predicted in 1870

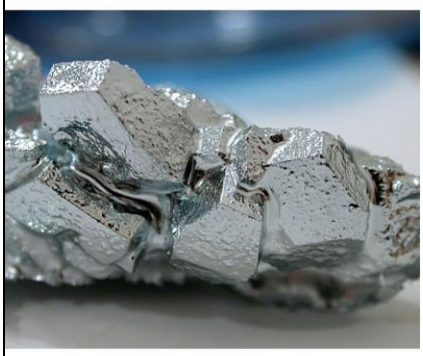


>In 1869, when he first assembled the Periodic Table of the elements, Dmitri Mendeleev noticed several gaps in the otherwise orderly arrangement of elements

>Right below Aluminum and Silicon were two yet-to-be-discovered elements. He named them eka-Silicon and eka-aluminum

>Mendeleev was even able to predict the physical and chemical nature of these elements

Gallium Metal



>He predicted that one of these elements – eka-aluminum - would be a shiny solid metal at room temperature

>And that it would melt below 30 degrees C, right in the palm of your hand

>Just four years later, Paul Emile LeCoq discovered this element and named it “Gallium”

http://en.wikipedia.org/wiki/File:Gallium1_640x480.jpg

Melting Point: 302.9146 K, 29.7646 °C, 85.5763 °F

Predicted as “eka-aluminum” in 1871 by Mendeleev

First identified in 1875 by Paul Emile Lecoq as existing naturally (as a salt) in zincblende ore [ZnS] by spectroscopic line in the blue

Some Historic Events for Compound Semiconductors

1871 – Mendeleev Predicts Existence of Gallium

1875 – LeCoq Discovers Gallium with Spectroscopy

1926 – Goldschmidt Synthesizes Gallium Arsenide

1947 – Invention of Ge Transistor ignites interest in Semiconductors

1952 – Welker Proves III-V Compounds to be Semiconductors

1955 – Gremmelmaier makes first GaAs device – A Solar Cell

- 51 Years from Discovery of Ga to synthesis of GaAs

- 29 Years from Synthesis of GaAs to First Device!

>Le Coq made very small quantities of Gallium and through the years there was very little demand for the stuff

>In 1926, geochemist V.M. Goldschmidt produced a number of III-V compounds, including GaAs

>But even then, in 1926, these compounds were merely laboratory curiosities

>But the 1947 invention of the transistor – based on Germanium (Mendeleev's eka-silicon) - ignited interest in III-V compounds

>The big question was: "Would these compounds be semiconductors, like their Column IV cousins?"

>In 1952 Heinrich Welker proved that indeed they were, and just 3 years later came the first compound semiconductor optoelectronic device – Gremmelmeier's GaAs Solar Cell

>It had been 51 years from the discovery of Gallium to the synthesis of GaAs, and another 29 years to the invention of the first GaAs electronic device.

1962 – A Big Year for GaAs Developments

Gunn Diode – First GaAs Microwave Frequency Device

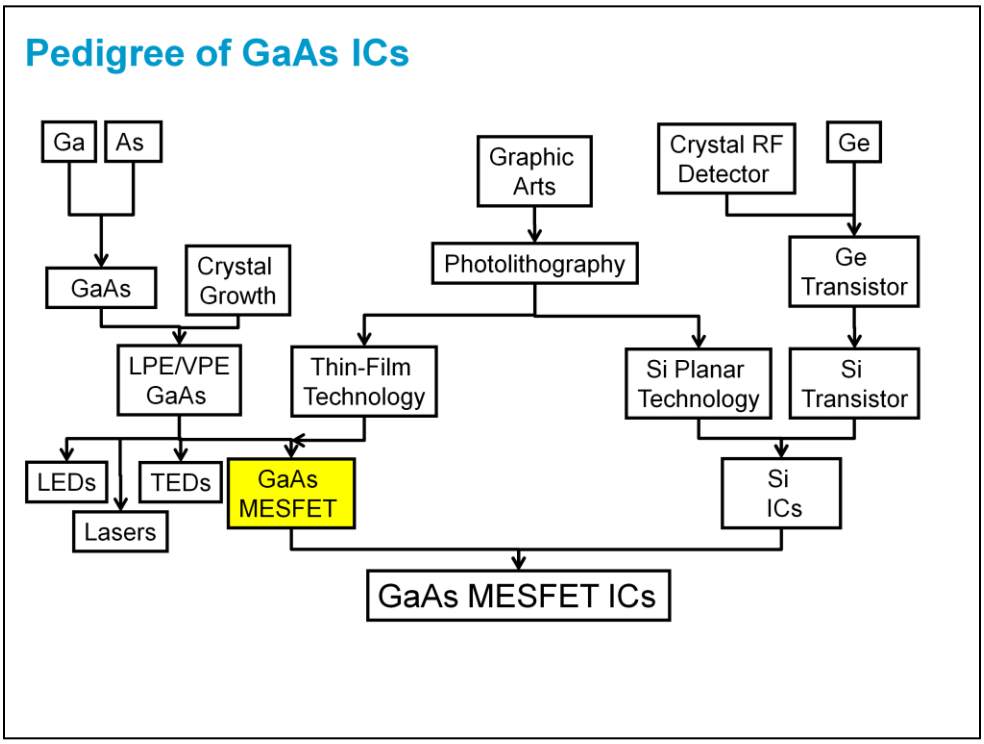
Visible GaAsP LEDs – Ancestor of Today's Multicolor LEDs

Semi-insulating Substrates – Foundation of 3-Terminal Devices

GaAs Laser – 850nm Infrared Emission

>From there, III-V developments came fast and furious

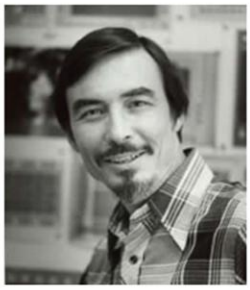
>1962 saw four major developments: the Gunn Diode; Visible GaAsP LEDs; Semi-insulating substrates, and the GaAs semiconductor laser.



>But still, GaAs had no 3-terminal amplifying and switching device

>In 1965 all that changed

1965 – Carver Mead Invents the GaAs MESFET



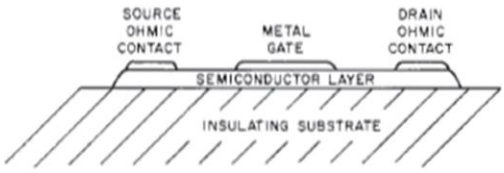


Fig. 1. Cross section of Schottky barrier gate FET.

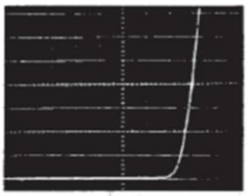
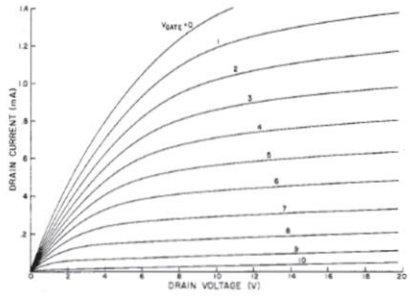


Fig. 2. I-V characteristic of gate-channel barrier. Horizontal: 0.2 volt/maj. div. Vertical: 10 μA/maj. div.

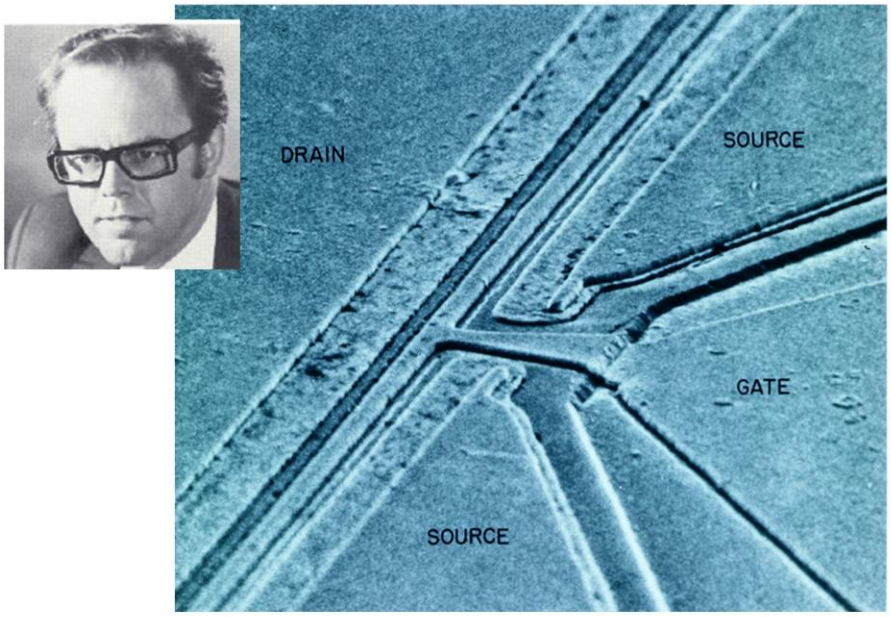


>In that year, Carver Mead of Cal Tech got hold of some epitaxial material from researchers at Texas Instruments

>He figured it should be easy to make a depletion mode FET using a Schottky barrier on GaAs as a gate

>Over the Thanksgiving holiday weekend in 1965, he got one to work, and because of that we are all meeting here today

1972: Charles Liechti Reports First HP GaAs FET

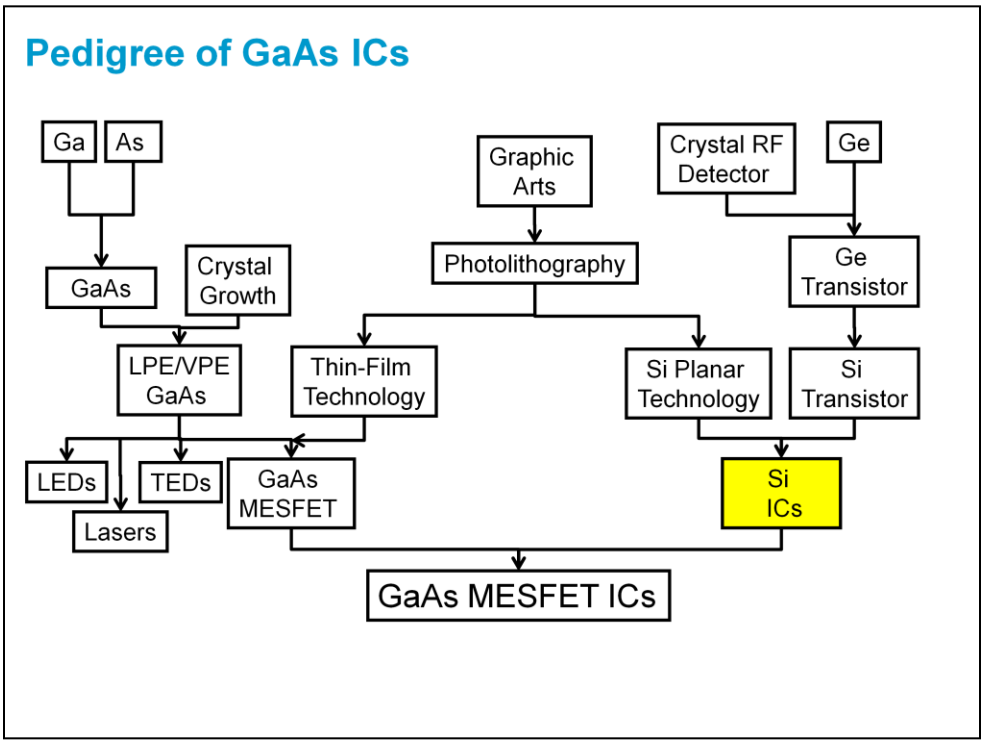


>Over the next 6 years, researchers worked to improve Mead's MESFET

>Not the first, but the most effective, effort was by Charles Liechti and his co-workers at Hewlett-Packard Labs

>In 1972, Charles reported a MESFET with 15GHz Ft, a record for the time

>At last, GaAs had what it needed: a 3-terminal amplifying device!



>Over on the other side of the family tree, things had been moving even faster

>Silicon had replaced Germanium as the material of choice for transistors

Noyce IC Patent
Filed 6/30/1959

"Semiconductor Device and Lead Structure"
[Based on Planar Technology Developed by Jean Hoerni]

April 25, 1961 R. N. NOYCE 2,981,877
SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE
Filed July 30, 1959 3 Sheets-Sheet 2

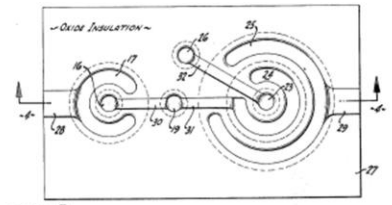


FIG. 3

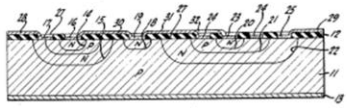


FIG. 4

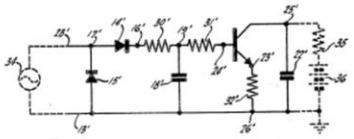
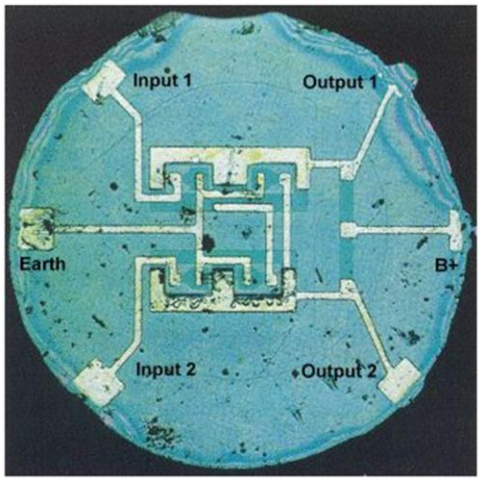


FIG. 5

INVENTOR.
Robert N. Noyce
BY Lippincott & Kalb
ATTORNEYS

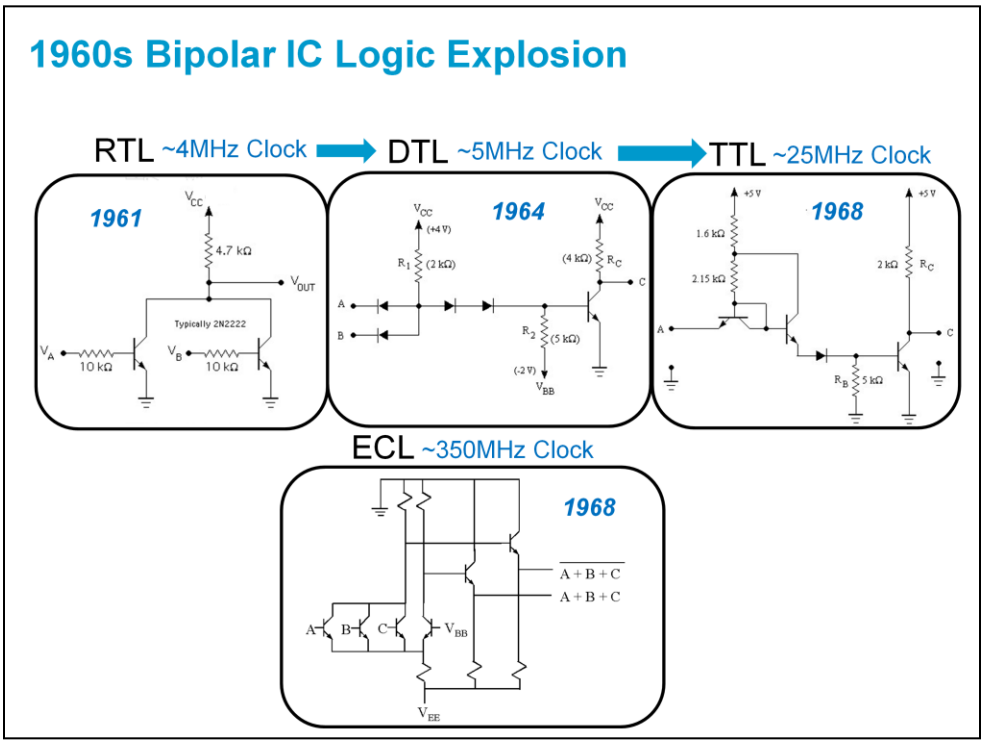
>And in 1959, Bob Noyce of Fairchild filed this famous patent application: "Semiconductor Device and Lead Structure" based on the Fairchild Planar Process developed by Jean Hoerni

Fairchild's First Monolithic Flip-Flop - 1961



1961: First Monolithic Silicon IC Chip. Invented by Robert Noyce, Fairchild

>And by 1961, Fairchild had reduced Noyce's patent to practice, demonstrating their first Silicon IC, a simple Flip-Flop: pretty isn't it?

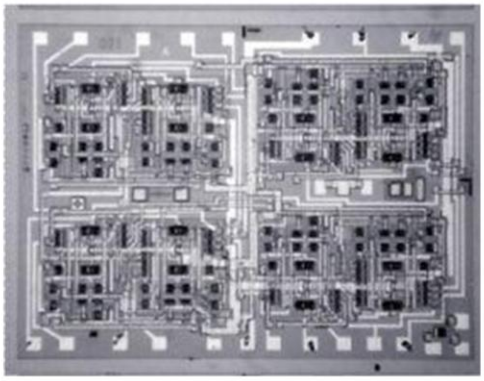


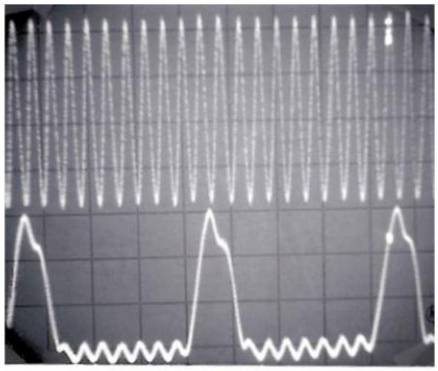
>This led to the Bipolar IC Logic Explosion of the 1960s

>This was a real revolution: 4MHz RTL, 5MHz DTL, 25MHz TTL and the speed champ: 350MHz ECL

>In my first job out of college, I built Instrumentation with this Fairchild and Motorola logic

500MHz ÷10 Counter…My First IC: Designed 1969

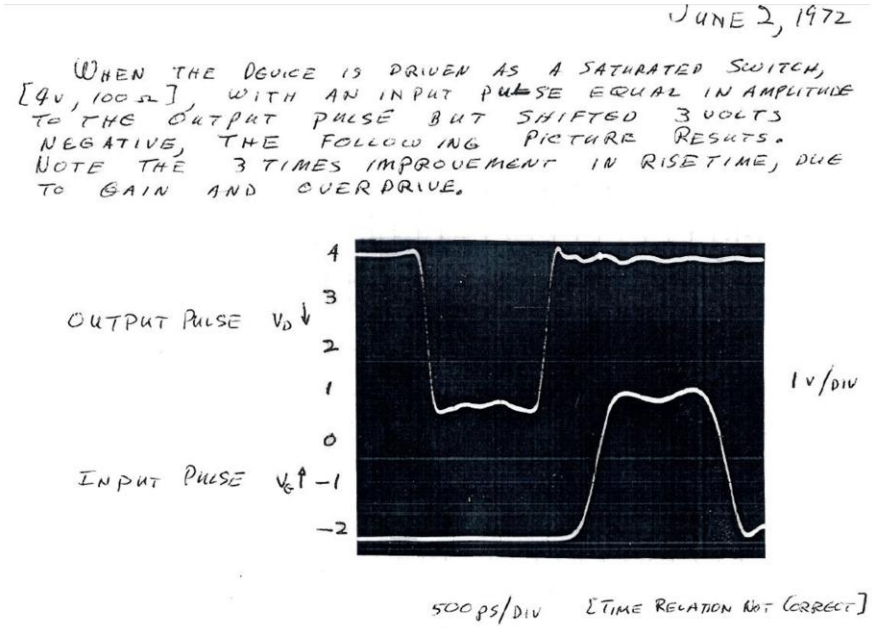




Note: 2GHz f_T Transistors!
1.25” diameter wafers

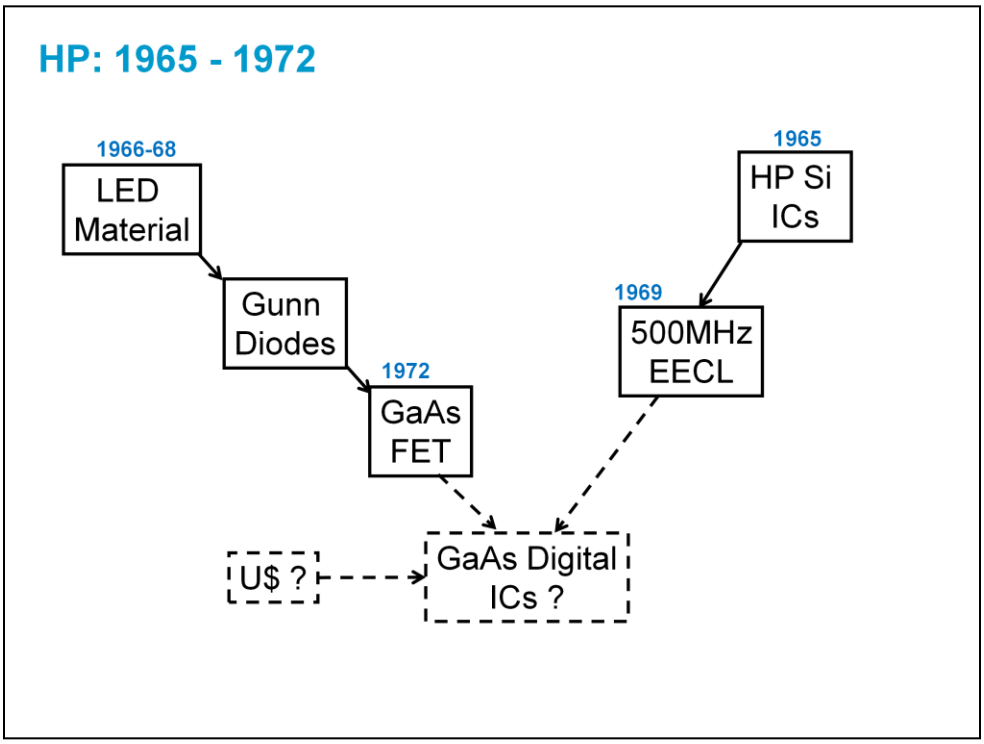
>And when I joined HP in 1969, I got to design and process this circuit – a 500 MHz divide-by-ten counter – in the blazing fast in-house proprietary Si bipolar process. **2GHz Ft! (**Before the end of my career, I got to design with compound semiconductor devices that had greater than 200GHz Ft).

First Test of GaAs FET as a Switch



>In 1972, I contacted Charles Liechti at HP Labs, got one of his GaAs MEFETs, and tested it for switching properties

>The thing looked great! Here it is, showing clean switching with about 60ps delay [there is a time offset between the traces]



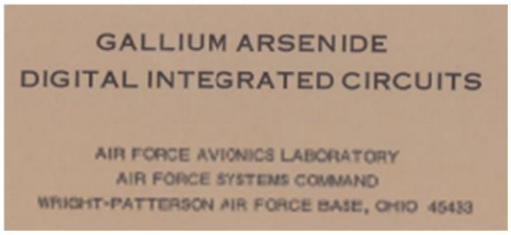
>So by 1972, the Gallium Arsenide and silicon branches of the family had converged at HP

>It was only a matter of time and money for GaAs Digital ICs to enter the world

>And the most reliable and far-sighted source of funds in those days was Uncle Sam

The Air Force Avionics Lab Contract

In September, 1972, I co-authored a Contract Proposal…



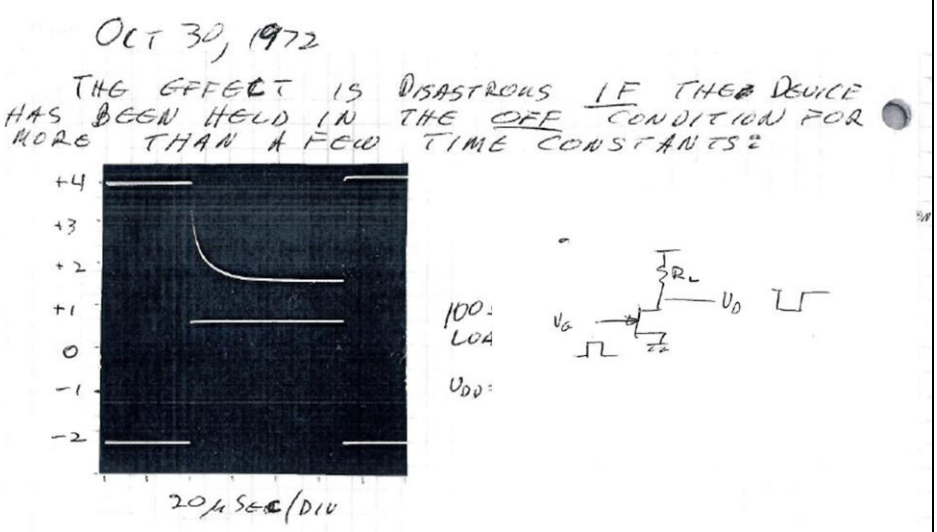
Then Transferred to HP Labs in hopes it would come through!

>All jazzed up about the possibilities, I volunteered to help produce a proposal for Air Force funding

>And soon after, I transferred to HP Labs, ready to make some GaAs ICs

>We got to work even before the hoped-for Air Force money came through

Disaster Strikes … The *Lag Effect*



>Right away, things fell apart

>I could now get plenty of FETs to test, but everyone of them was a dog!

>The devices would switch OFF just fine

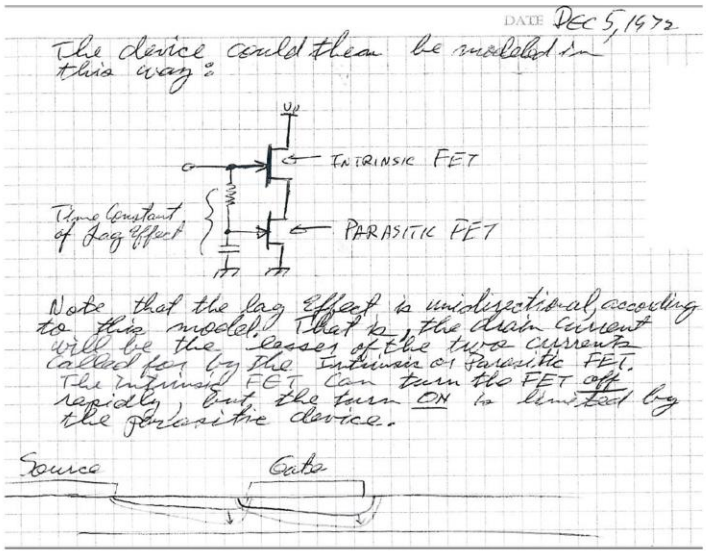
>But they would switch ON only about 25% of the way before leisurely coasting to a stop tens of microsecond later

>In my grief and frustration, I named this the “Lag Effect”

>I really think that had that first sample I tested back in June shown this effect, I would have said goodbye and good riddance to GaAs

>To this day, I still do not know why that first device behaved itself. Perhaps it was some kind of a cosmic joke? Who knows?

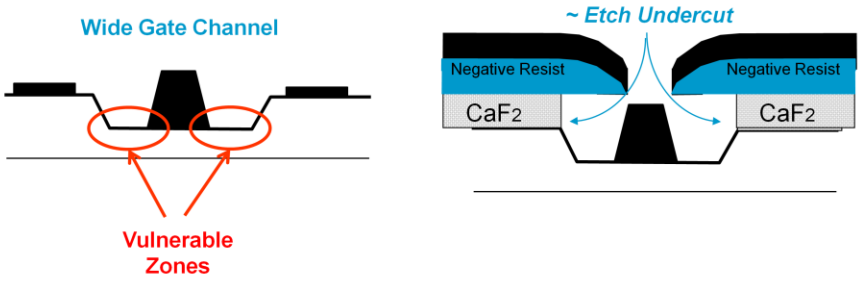
A Simplified *Lag Effect* Model



>You could think of the Lag Effect this way: a fast FET in series with a slow FET

>This implied that surface states must have been the villain

MESFET Channel Geometry 1972-73



Quick Fix: Extreme Care in Gate Processing

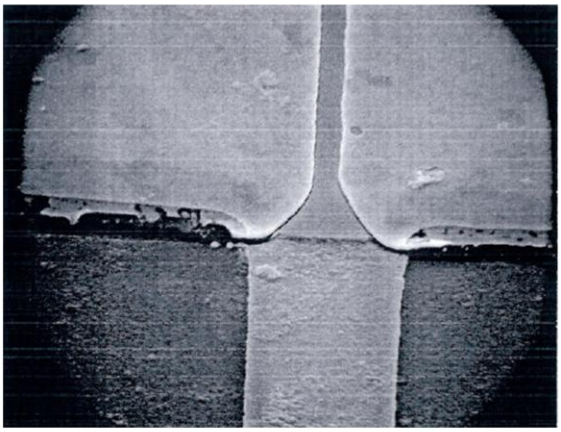
Permanent Fix: Change the Process!

>The MESFETs had been processed using a Calcium Fluoride gate lifting assist layer

>This gave a clean lift, but the etch undercut left wide expanses of exposed channel where surface depletion could do its dirty work

>What we needed was a bulletproof way to eliminate this etchback

Self-Aligned Gate: Lag-Free, But Impractical



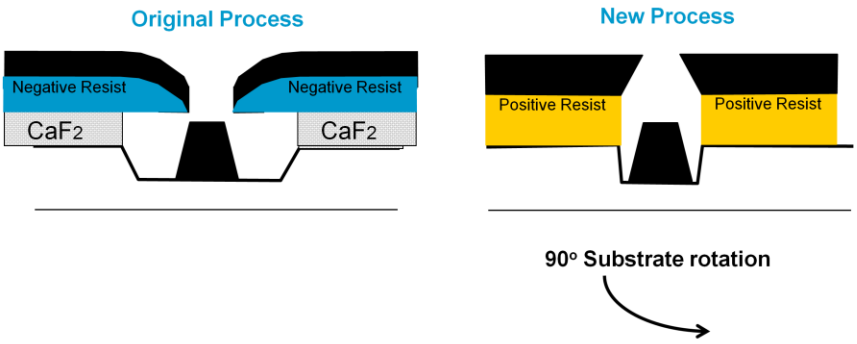
Self-Aligned Gate Removed Lag but was plagued by shorts

>We tried a self-aligned process, where source and drain contacts defined the gate.

>Lag effect was completely eliminated, but yield was terrible because filaments of gold shorted gate to source and drain

>Close, but no cigar

Channel Process Modification - 1974



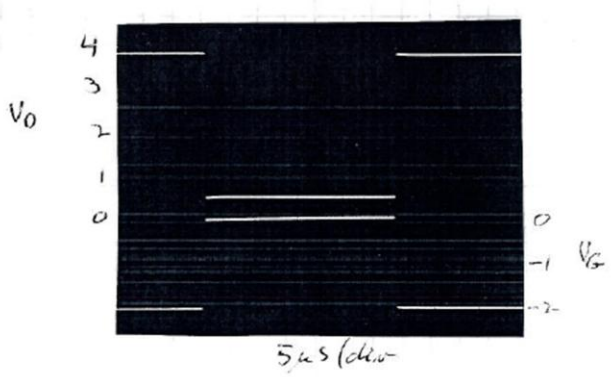
>So we limped along through 1973 with the original process, being very careful to minimize the undercut as much as we could

>It wasn't until 1974 that we were able to implement a simple process change that eliminated the Calcium Fluoride

>We also rotated the substrate 90 degrees to get sharper trench walls with less undercut

>**If** we were very careful – and very lucky – this process could do the job

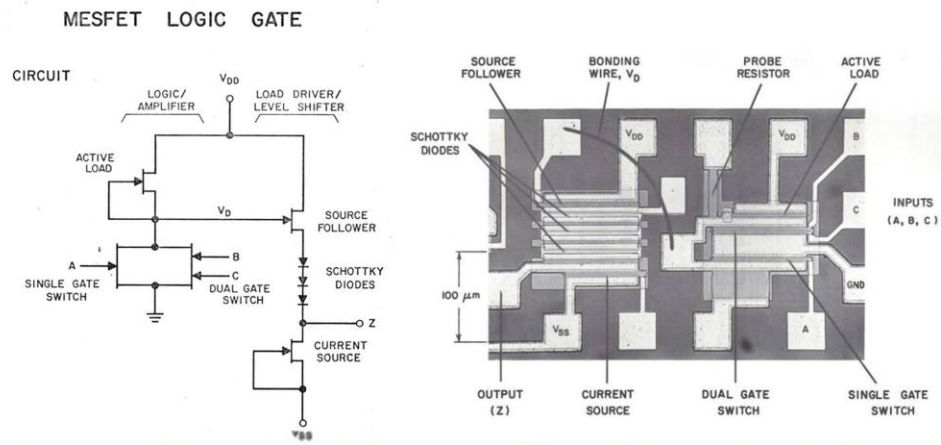
Lag Effect Finally Conquered…April, 1974



- *Rotate Layout 90° to Get Sharper Etch Walls*
- *Switch from Indirect to Direct Gate Metal Liftoff*

>By early 1974, we had finally subdued the Lag Effect

The First GaAs MESFET Monolithic IC - 1973



Designed December, 1972 *Tested September, 1973*

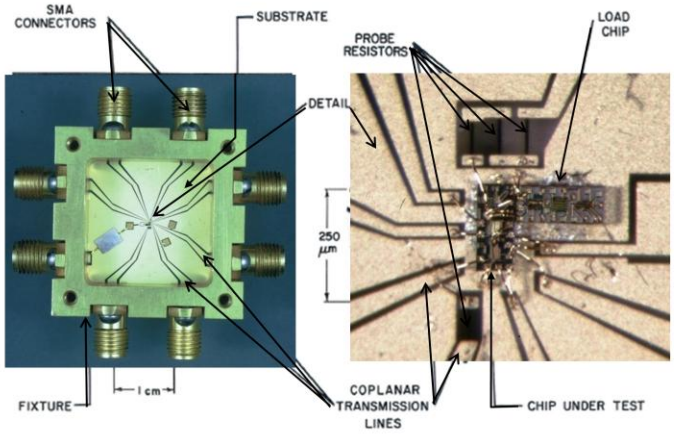
12 Years After First Silicon IC

>In 1973, using the original FET process, we built this simple logic gate

>Here it was at last, an actual monolithic GaAs IC

>At this point, Gallium Arsenide was 12 years behind Silicon in the Digital Circuit derby

Coplanar Waveguide Test Fixture - 1973



>To test this circuit, I built this test fixture using coplanar waveguide [CPW], a relatively new transmission line technology at the time.

>The CPW enabled me to get signals close to the chip in a 50 ohm transmission line.

>By mounting a second chip behind the chip under test, I was able to measure the propagation speed with different loads.

It was Fast Logic for 1973

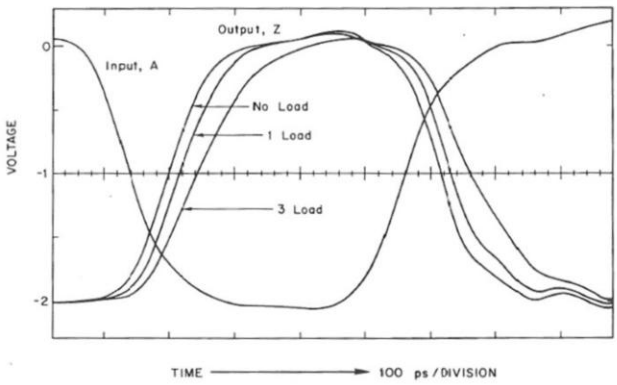


FIGURE 6—Pulse response of MESFET logic gate. Delay with no load = 60 ps, with one load = 75 ps, with three loads = 105 ps.

>The results were impressive for the time.

>Propagation delays were 60ps unloaded, 75ps with a fanout of 1, 105ps with a fanout of 3.

>This offered the prospect, for the first time, of multi-GHz clock rates

Challenges in 1974

Miniaturize the Gate Layout

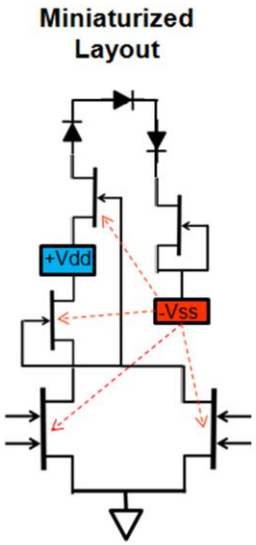
Improve the Yield

Make Useful Demonstration Circuits

>But a lot of hard work lay ahead.

>We needed to miniaturize the layout, improve the yield, and make some useful demonstration circuits.

Miniaturized Layout Suffered Sidegating Effect



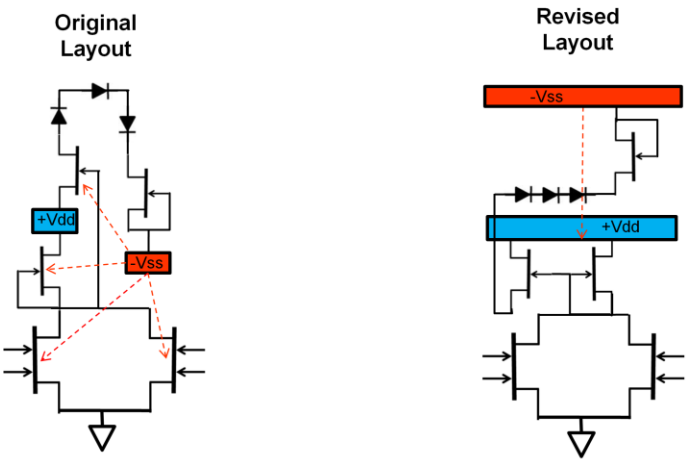
>It was easy enough to miniaturize the layout, but this caused some problems

>One problem was a form of backgating we eventually called sidegating

>The most negative potential in the circuit changed the pinchoff of FETs throughout the circuit

>Each FET's pinchoff was affected differently, depending on its distance from the Vss terminal and its average gate potential!

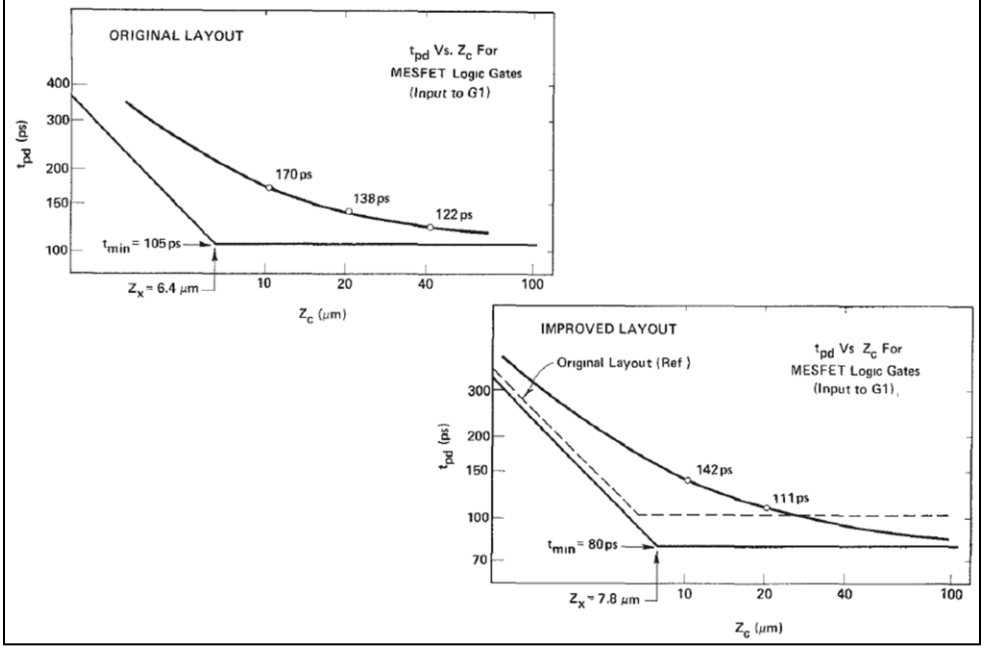
Revised Layout Reduced Sidegating Effect



>In the second iteration, I papered over this problem by changing the layout configuration

>This problem would not be solved until years later, in the production process, with the introduction of proton isolation.

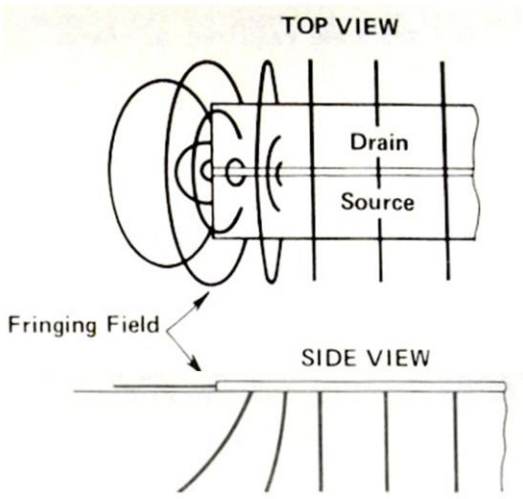
Parasitic Capacitance Slowed Miniaturized Logic



>Another problem was the slowdown of circuits with the miniature layout

>As the width of the FETs was scaled down to reduce power consumption, the propagation delay increased

Parasitic Capacitance End Effect

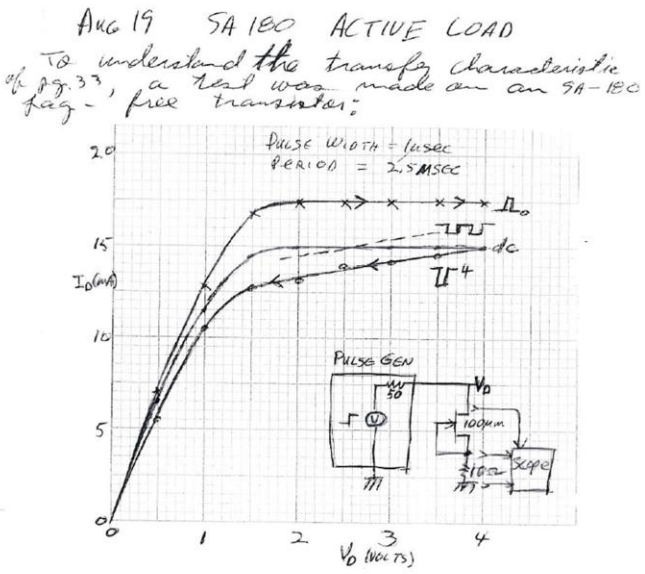


>This was due to fringing fields at the end of the FETs

>Until we could shrink the contact sizes in proportion to the gate width, this would remain a problem

>So, not surprisingly, there was a speed-power tradeoff

No Lag, but Plenty of Hysteresis…



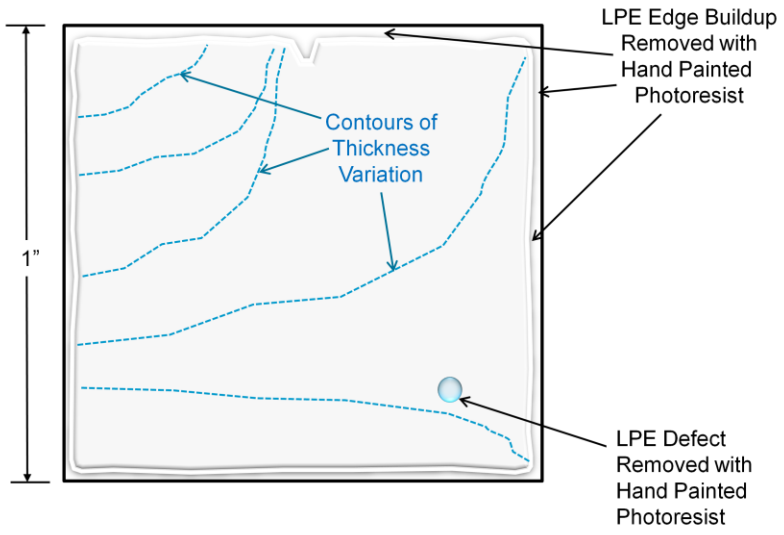
>Although we had pretty much put the Lag Effect to bed, there was another device anomaly to contend with.

>It came to be cursed by many epithets:" Drain Transients", "Hysteresis", "Slow Tails", "Looping"

>Changing Vds, even with constant Vgs, caused a time-dependent overshoot in drain current

>This effect would frustrate every circuit designer who ever tried to work with GaAs MESFETs

The GaAs LPE Wafer 1972 - 1977



>Another problem was the material itself

>The conductive layer technology we used was inherited from LEDs: Liquid-Phase Epi, or “LPE”

>“LPE worked sort of like spreading peanut butter on a slice of bread”

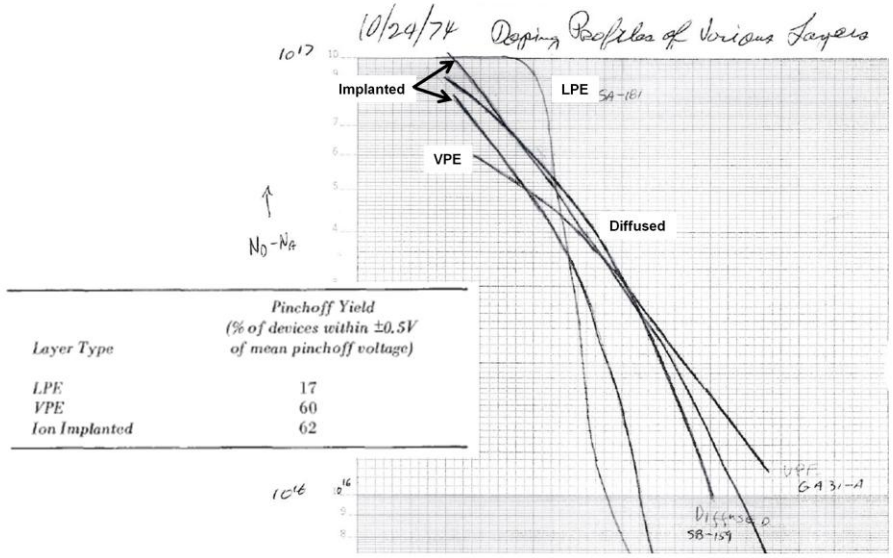
>The layers were non-uniform and full of defects

>AND – get this- LPE demanded Square Wafers

>For those of you who have never had the pleasure of processing square wafers…count yourselves most fortunate!

>But the worst thing about LPE was the lousy pinchoff uniformity

Experiments: LPE, VPE, Diffusion, Implantation



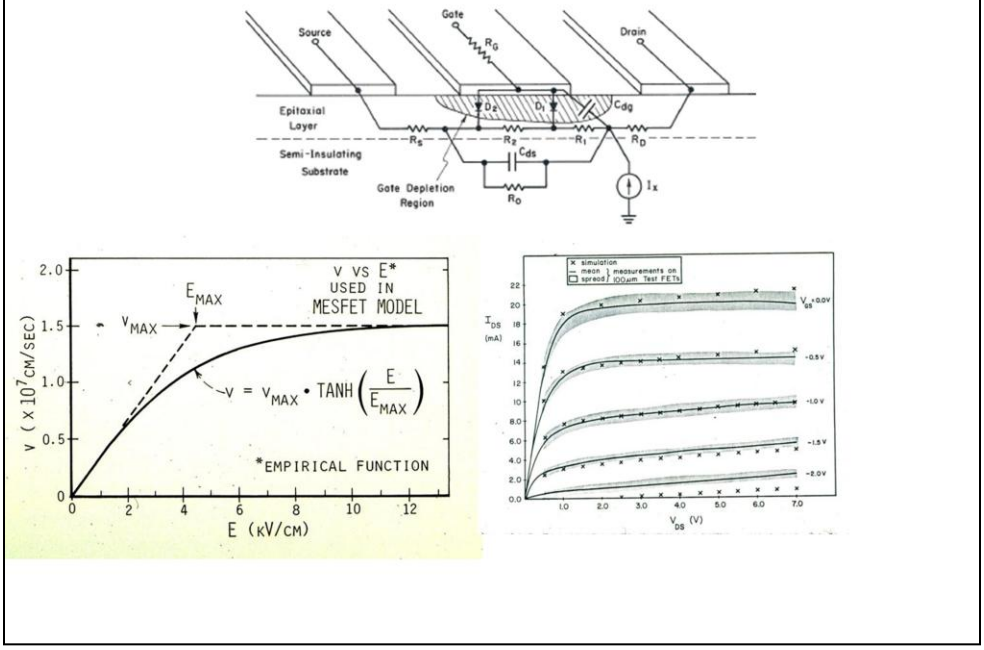
Layer Type	Pinchoff Yield (% of devices within ±0.5V of mean pinchoff voltage)
LPE	17
VPE	60
Ion Implanted	62

>If we wanted pinchoff variations of less than 1 volt, we had to accept a 17% yield with LPE

>So we investigated Vapor-Phase Epi, Diffusion, and Ion Implantation into undoped LPE buffer layers

>Ion implantation gave the best results, so from the moment we got it in late 1974, it became our standard n-layer

The Non-Linear Device Model – HP Minicomputer



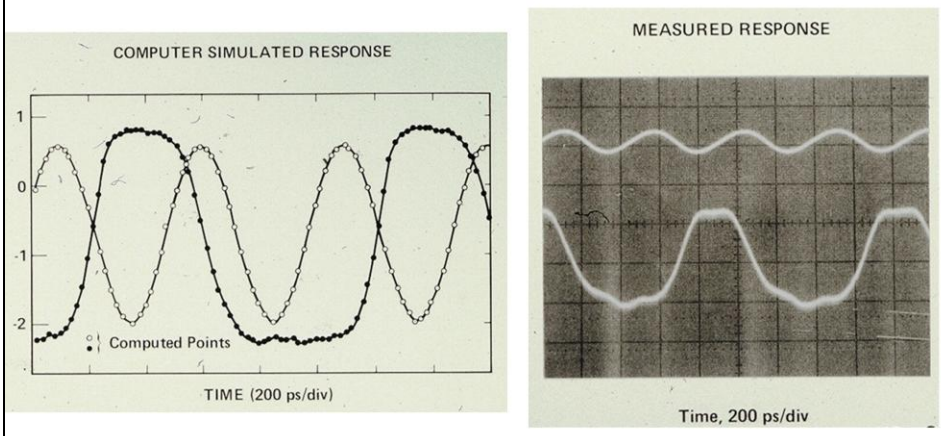
>If we wanted to do any kind of speculative circuit design, we would need a device model for CAD

>In 1973 I had developed a simple two-lump non-linear MESFET model based on a mixture of simple theory and empirical formulas

>In the early stages, the model took lots of time to develop on a mini-computer and didn't produce any useful results.

>But by late 1974 I was able to get some believable results with it. By that time I had ported the model to a circuit design program that ran on the Corporate IBM mainframe.

1975 Circuit Simulation on IBM Mainframe



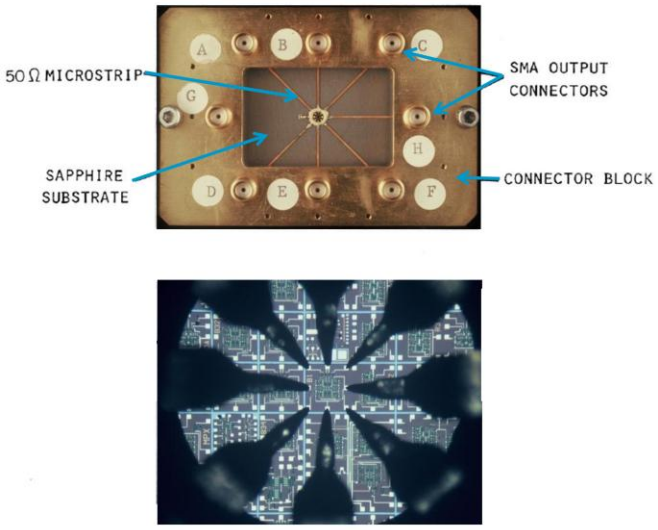
>But by 1975, the model was yielding useful results and predictions

>I had to submit the simulation job as a deck of IBM punched cards, and get the output on fanfold paper from the line printer. If the printout was thick, I knew the job had run. If it was thin, I knew I had made a syntax error and the mainframe had spit it out

>Near the end of every month it was impossible to get job turnaround, since the HP payroll was being calculated and printed on that very same IBM mainframe!

High Speed IC Probe Card

…….(Developed at HPSCD)

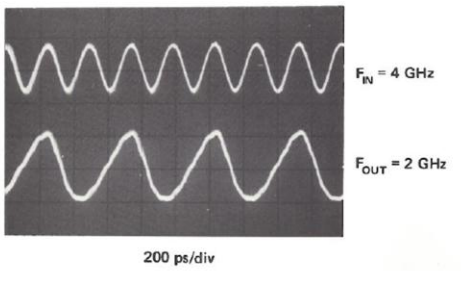


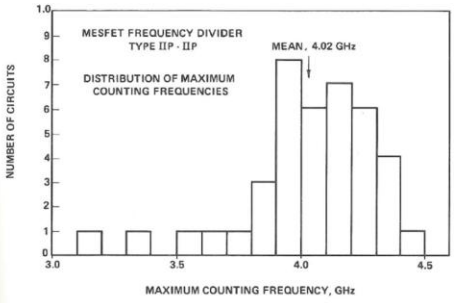
>Another useful tool was one I had helped develop at HP Santa Clara, and brought to the Labs

>It was the high-speed probe card I had used to test 500MHz Silicon ICs

>It worked just fine up to at least 4GHz

1976: A 4GHz ÷2 Counter

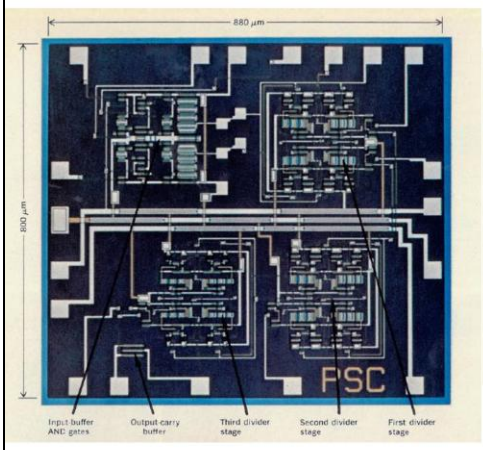


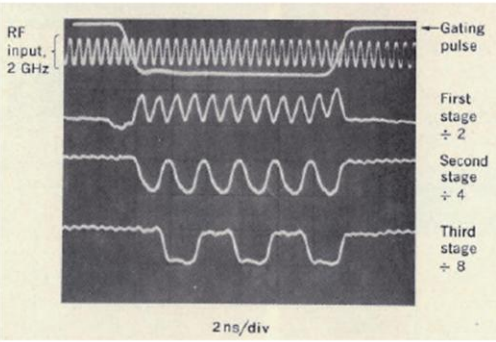


>With Ion-implantation, lag-free gate processing, miniature layout, improved circuit design and on-wafer testing we were by 1976 finally able to get some really encouraging results

>A simple divide-by-two circuit toggled at 4GHz, a record for the time

1976: A ÷8 Counter





>A gated divide-by-eight counter operated with 2GHz clock.

1976: An 8x Multiplexer

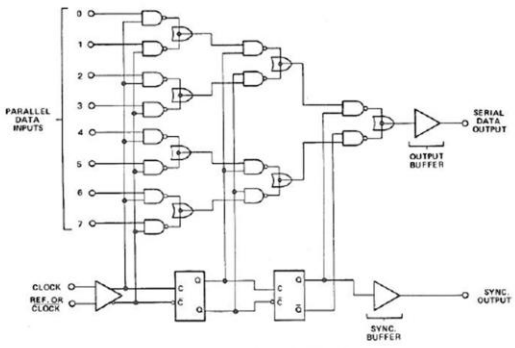
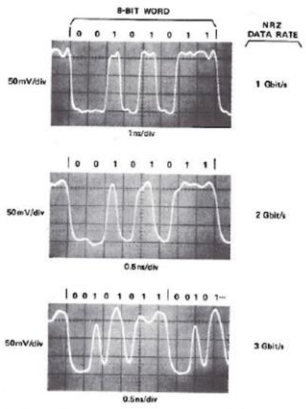


Fig. 11. Logic diagram of an 8-bit multiplexer/data generator.



12. Multiplexer/data generator operating at nonreturn-to-zero data rates of 1, 2, and 3 Gbit/s.

>And a very rudimentary 8:1 Multiplexer could be coaxed up to 3Gigbits per second

Key Contributions of 1974 - 1976

- Solved the *Lag Effect*
- Miniaturized the Layout
- Dealt with *Sidegating* and other Substrate effects
- Applied the MESFET Computer Model
- Replaced LPE with Ion Implantation
- Built MSI Circuits with Clock Rates as high as 4GHz

>By the end of the Air Force contract, we had

•Solved the *Lag Effect*

•Miniaturized the Layout

•Dealt with *Sidegating* and other Substrate effects

•Applied the MESFET Computer Model

•Replaced LPE with Ion Implantation

•Built MSI Circuits with Clock Rates as high as 4GHz

The Situation in 1976

Practical Medium-Scale GaAs Logic had been Demonstrated

Just 10 Years After Invention of GaAs MESFET and

20 Years After First GaAs Electronic Device

BUT…

By This Time Silicon Microprocessors Had Been on the Market for 4 Years!

Clearly, GaAs Digital ICs Were Headed for a Niche.

If they were to survive, GaAs ICs would need to be branch out!

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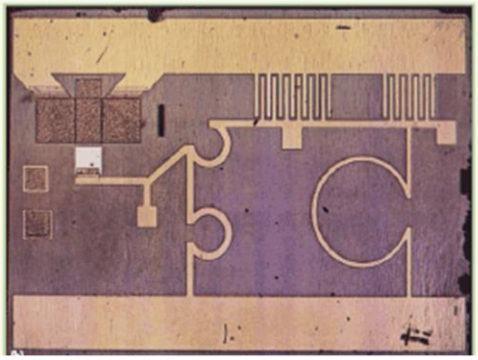
If they were to survive, GaAs ICs would need to be branch out from the digital enclave!

Plessey's First MMIC, an X-Band LNA [1974-75]



One Grounded-Source FET + Passive Matching Elements

>One important branch of the GaAs IC family emerged in 1974-75

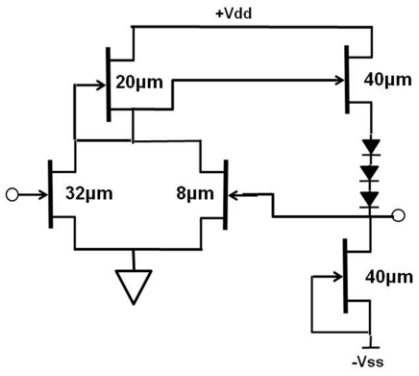
>Ray Pengelly of Plessey built a very simple circuit with a single MESFET combined with passive elements

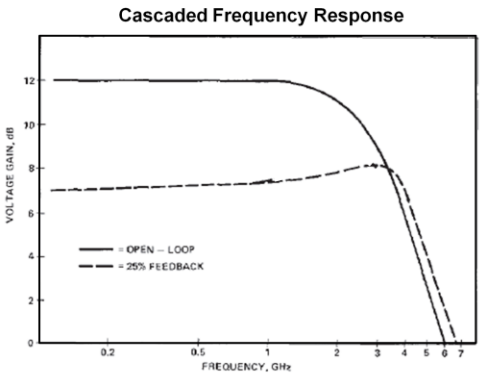
>As far as I know, this was the first of what came to be called MMICs

Designed 1974, published 1975

Pengelly, R. S., "Broadband lumped-element X band GaAs f.e.t. amplifier," Electron. Lett., 6 February 1975, pp.58–60.

DC – 4GHz Broadband Amplifier Cell - 1976

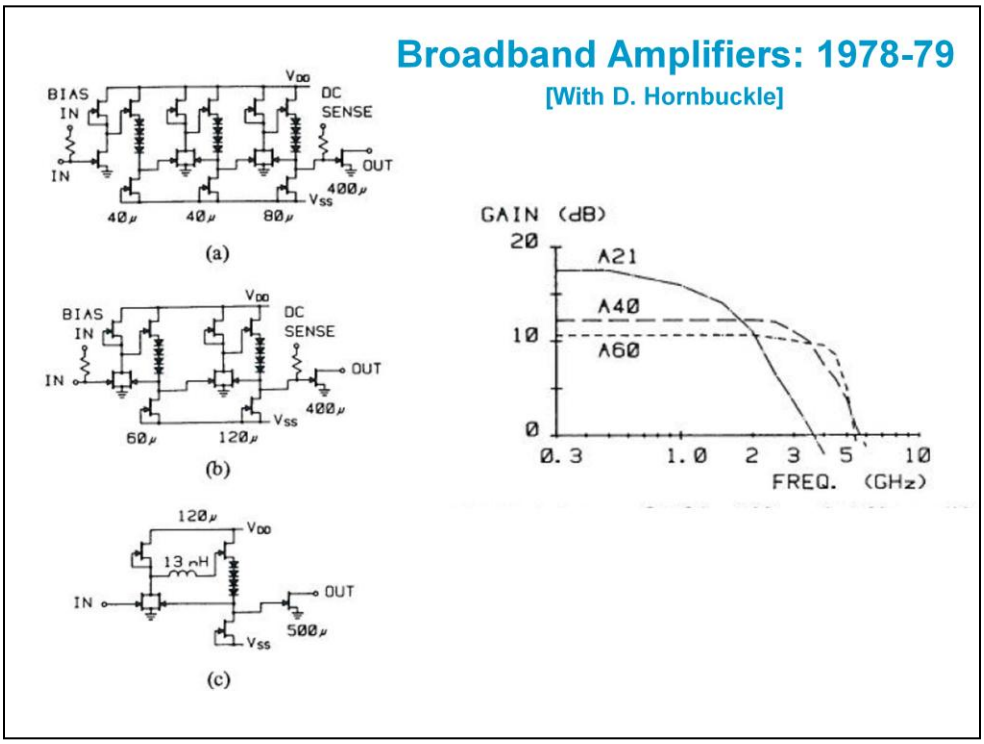




>In 1975-76 I had put a simple dc-coupled broadband amplifier test cell on our last digital mask during the Air Force contract

>With 25% negative feedback we got cascadable bandwidth in excess of 4GHz, a record for the time.

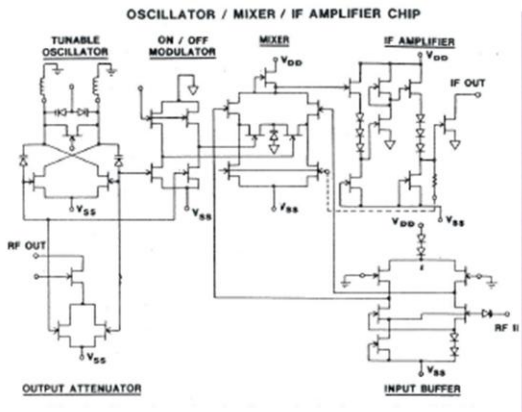
>With the end of our Air Force contract, I transferred to HP Santa Rosa, where the microwave instruments were made and GaAs FETs were going into production

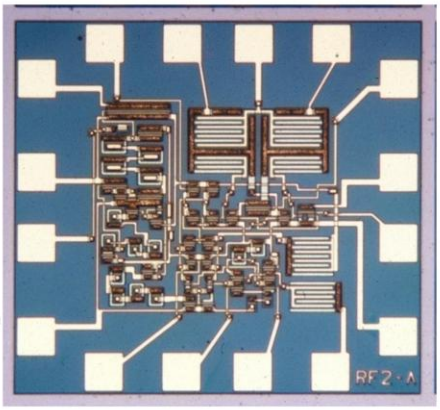


>There, I teamed up with Derry Hornbuckle to design several circuits, among them these broadband GaAs FET amplifiers.

>DC –to- 5GHz IC amplifiers were a novelty in those days.

The GaAs FET RF Signal Generation Chip [1978-79]





>The most complex circuit from that period was this GaAs FET RF Signal Generation Chip.

>I designed this circuit - consisting of a VCO, balanced mixer, IF amplifier and support circuitry - in an attempt to lower the cost of a proposed signal generator.

>The signal generator project was cancelled

>But the circuit was innovative for the time and I got to publish it in 1980.

Now it Was Time to Get Serious About the Process

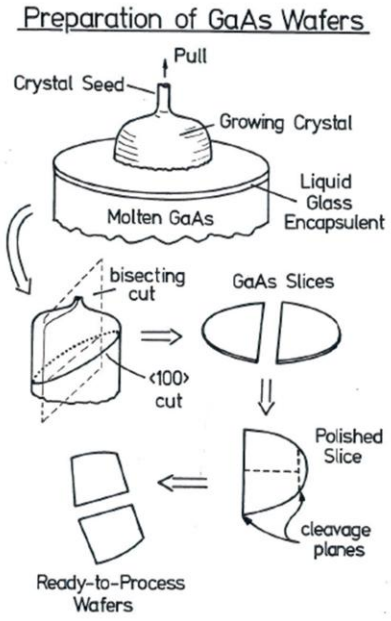
- All circuits to date had been built with HP Labs Process
- This Process was Unsuitable for Production
- In 1979, I transferred to Santa Rosa Technology Center to Lead the process Development Effort
- Infrastructure was In Place for Producing Discrete FETs
- We even Had a Fledgling LEC Crystal Growth Effort!

>With the demonstration of these various circuits, it became clear that we had to have a decent production-worthy process

>I was assigned to lead the team that would develop this process in the Santa Rosa Microwave Technology Center

>Here are the highlights of that process, developed in 1979-1981

The First GaAs IC Production Process



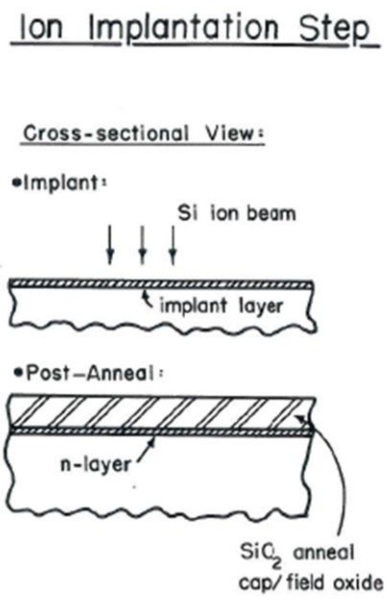
>Fortunately, we had a group that grew GaAs crystals with the Liquid encapsulated Czochralski method

>Initially, the wafers were cut into a squarish shape, as shown

>the big advantage of these crystals was that with the right stoichiometry control you could get something called the EL2 level

>This was a deep trap that rendered the substrate semi-insulating without the need for chromium doping

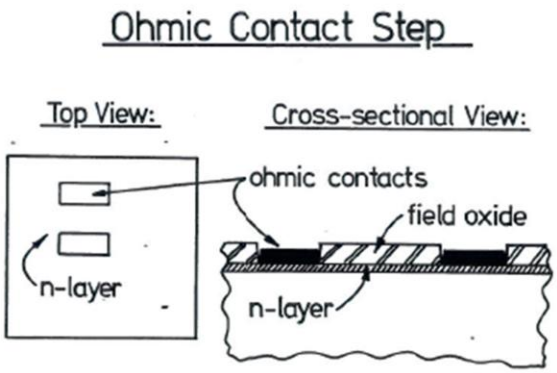
The First GaAs IC Production Process



>This in turn meant you could implant directly into the substrate. No epitaxial buffer layer was required, like we had done at HP Labs

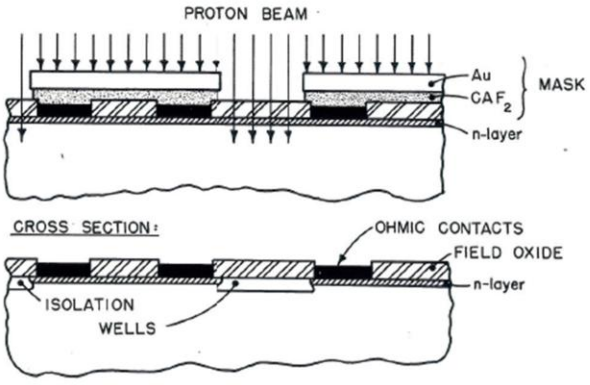
>We capped the silicon implant with low pressure CVD oxide for anneal

The First GaAs IC Production Process



>Then left that oxide in place to assist with metal lifting in all stages of the process, starting with the ohmic contacts

The First GaAs IC Production Process

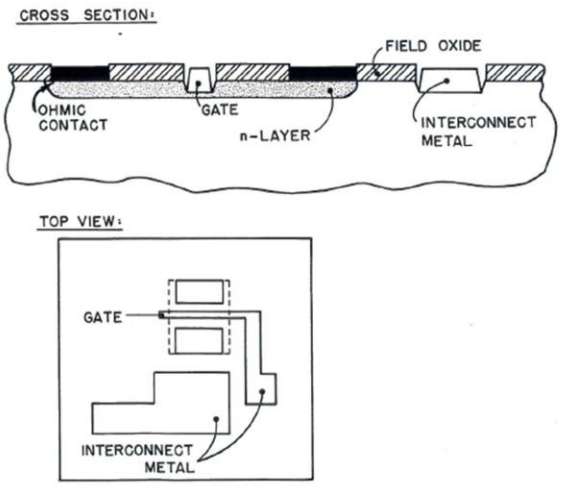


>The key to this process was proton isolation, developed by Don D'Avanzo

>This for the first time gave us a purely planar surface: no Mesa isolation !

>And, for all practical purposes, it killed sidegating once and for all

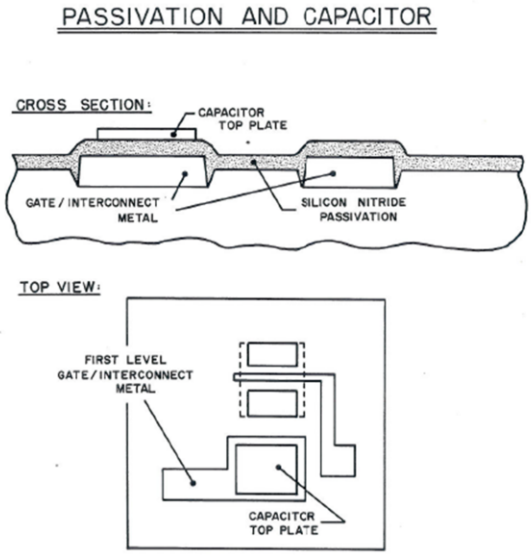
The First GaAs IC Production Process



>Lifted gate metal also served as first-level interconnect metal

>No Mesas to cross!

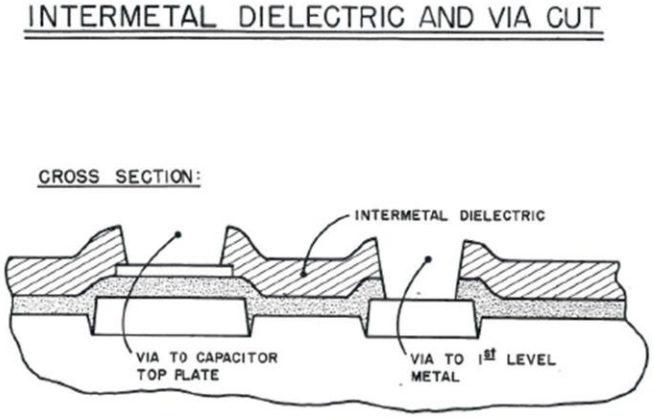
The First GaAs IC Production Process



>And the FETs were passivated by Plasma CVD silicon nitride

>This nitride doubled as a dielectric for thin-film capacitors

The First GaAs IC Production Process



>The process had two layers of interconnect metal

>The intermetal dielectric was something quite new at the time: spin-on polyimide

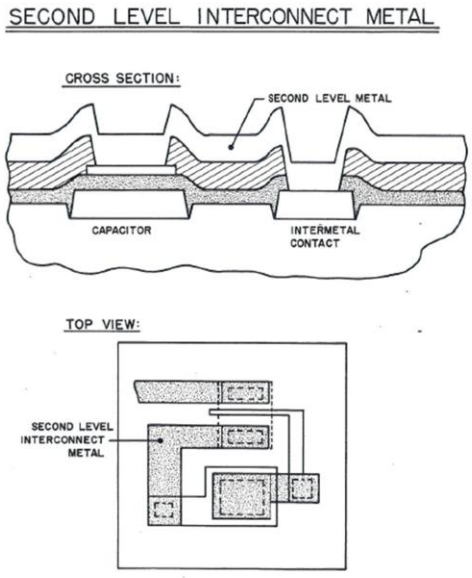
>We ion-milled vias through the polyimide down to the first metal layer and the capacitor top plate

>Milling stopped on the capacitor top plate, which was titanium

>While it punched right through the polyimide and nitride to make contact to the first level metal

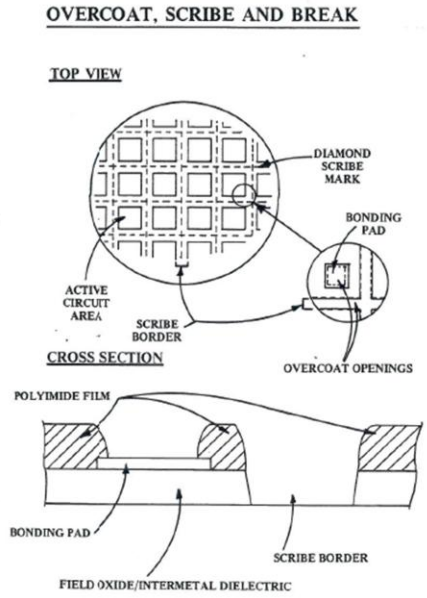
>Two contact levels in one step!

The First GaAs IC Production Process



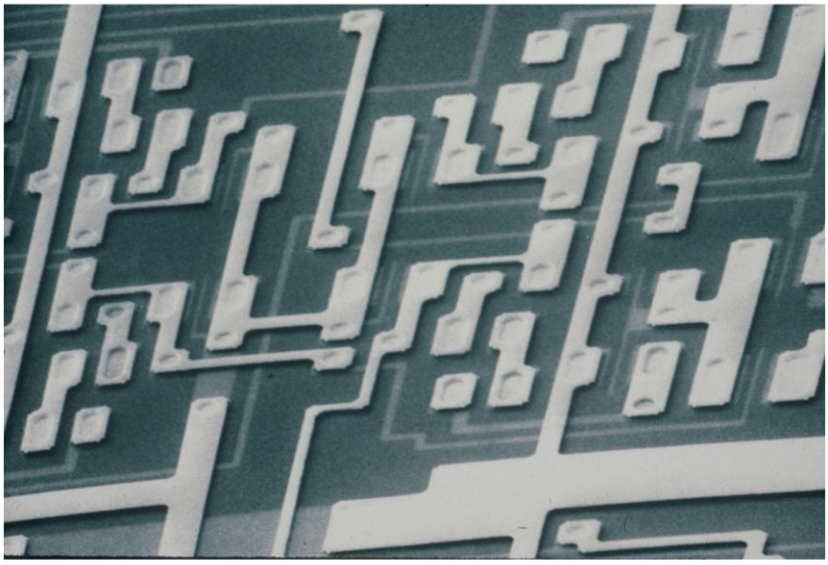
>The second metal was deposited over everything, then ion-milled for patterning

The First GaAs IC Production Process



>And finally a second coat of polyimide overcoated the chip and defined the chip separation border

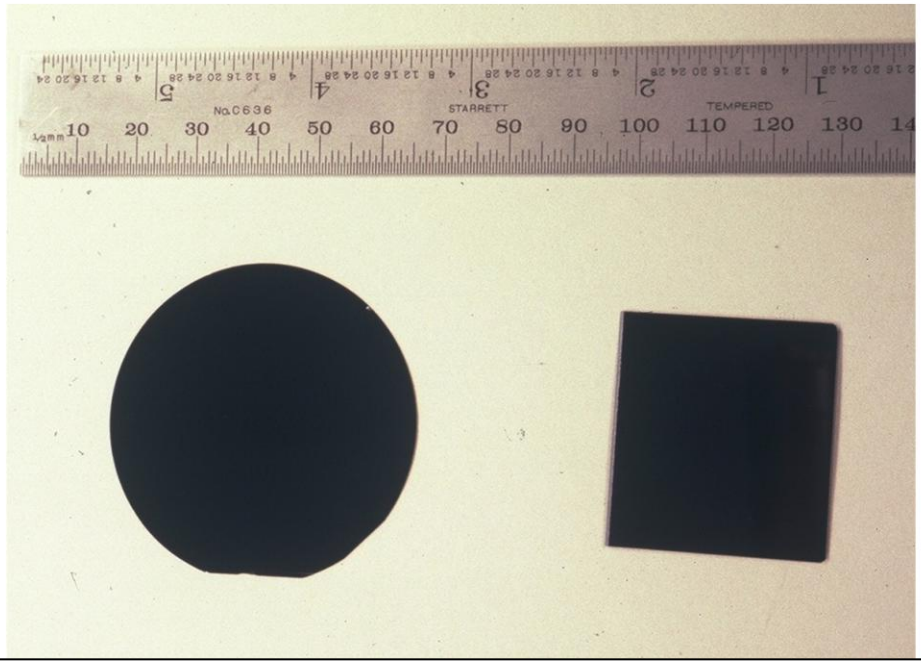
A Planar GaAs IC Process At Last!



>Thanks to the efforts of a hard-working team of engineers and technicians, by 1981 we had a fully-planar GaAs IC process

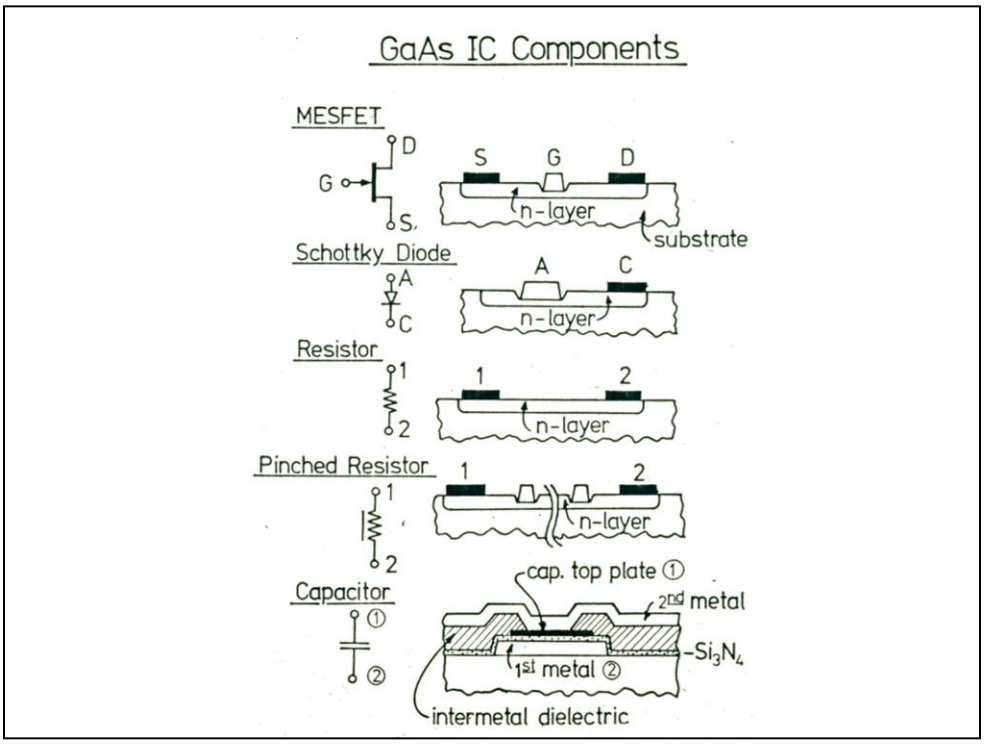
>Which we published at this conference in 1981

1981 – Round Wafers at Last!



>And toward the end of the project, in 1982, we even made some homebrew round wafers, the first at HP Microwave Tech Center

>Round wafers soon became commercially available and the industry kissed the square wafer goodbye



>We offered designers a process with these components:

>MESFET

>Schottky diode

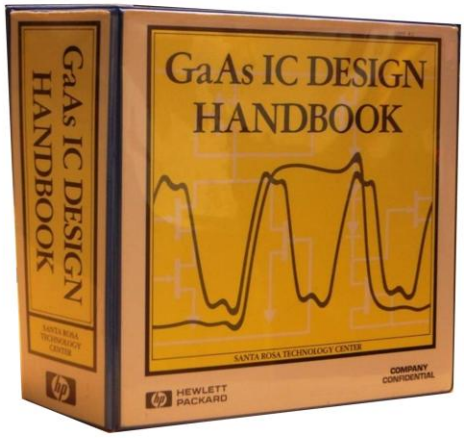
>Resistor

>Pinched Resistor

>And Capacitor

The Design Guide

…A Group Effort Edited by Don Estreich



>And documentation about the process and how to design with it

1986 – 1990 Product Shipments

Numerous Custom GaAs ICs were Designed by HP Engineers in the 1980s. By 1990, ***24 of these ICs had shipped in HP Instruments.***

Instruments included:

Frequency Counters

Signal Generators

Spectrum Analyzers

Active Probes

Arbitrary Waveform Synthesizers

Digitizing Oscilloscopes

Pulse Generators

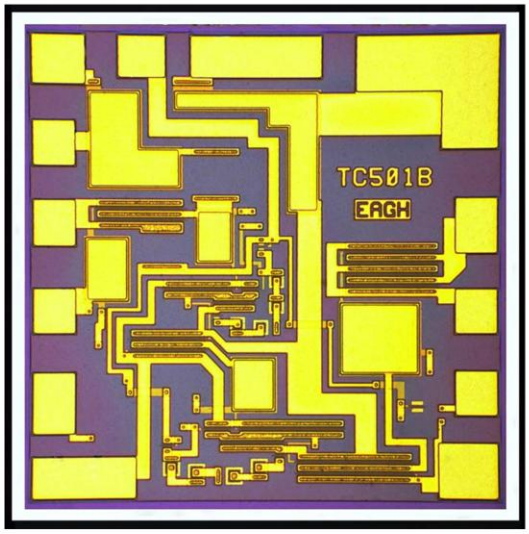
>So what did these designers do?

>After I left GaAs IC development, things really started to move forward

>The 1980s at last saw in-house custom designs for all these kinds of HP instruments

>Here are some examples of HP's GaAs ICs built with this RFIC process in the 1980s

80MHz – 3GHz Low Noise Amplifier



>One of our first ICs in the new process, this 80MHz to 3GHz amplifier was designed by Don Estreich in 1980 and finally shipped in 1986

TC-501 (LN1E)

Description: .08 – 3 GHz amplifier

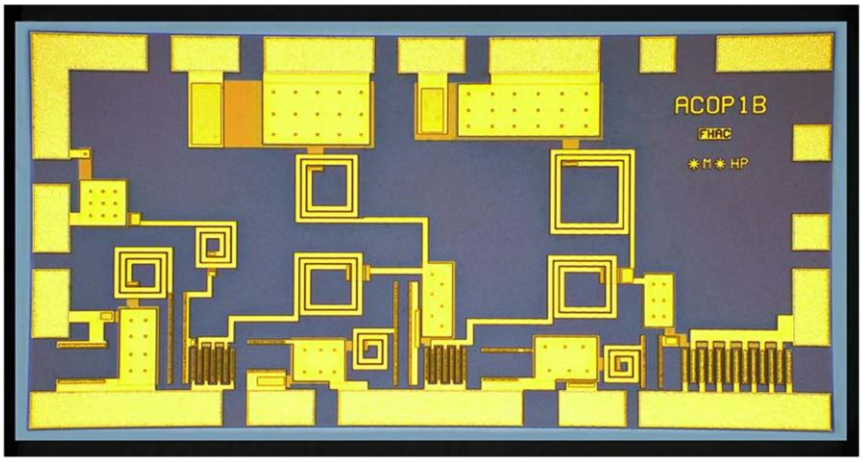
Designer: D. Estreich

Year Designed: November 1980 through March 1981

Year Shipped: 1986

Shipped in [instrument]: HP 5386A Frequency Counter (3 GHz) [2ea, along with TC-502 prescaler]

2GHz – 7GHz Output Amplifier



>This 2-7GHz output amp designed by Dennis Derickson also shipped in 1986
>It replaced an expensive hybrid circuit
>When this IC took over, an entire hybrid microcircuit assembly line was shut down

TC-503

Description: 2-7 GHz amp (ACOP1B)

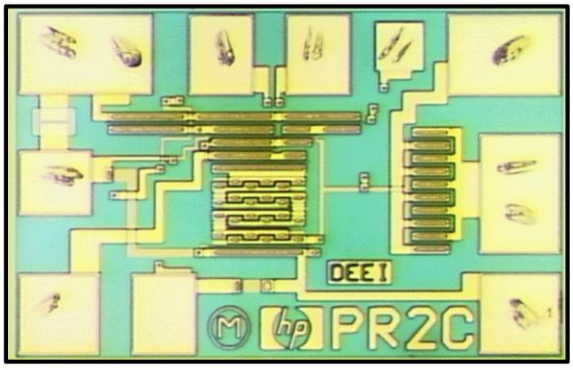
Designer: Dennis Derickson

Year Designed: 1985?

Year Shipped: 1986?
Shipped in [instrument]: 8671,2,3 Synthesized Signal Generators

Per John Imperato, who put it into production: “The amp worked great, but unfortunately displaced an entire line of hybrid microcircuit assemblers.”

HP 85024A 300kHz – 3GHz Active Probe VGA



>This nifty active probe amplifier by Derry Hornbuckle featured an on-chip spark gap for input overload protection

TC-509

Description: Variable gain 0.05 -3 GHz amp

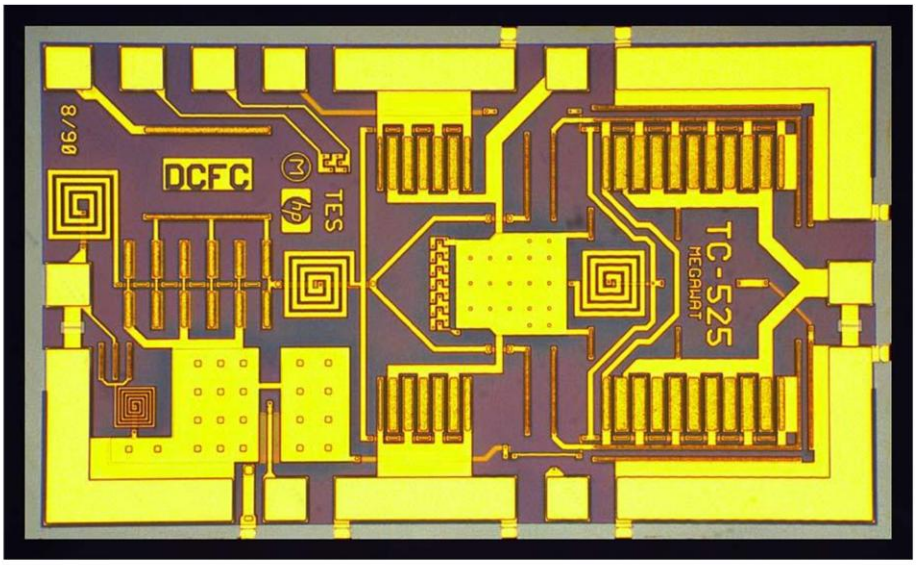
Designer: D. Hornbuckle (Derry designed it, Tim Shirley released it to production in ~1988)

Year Designed:

Year Shipped: 1988

Shipped in [instrument]: 85024A High-Frequency Active Probe, 300 kHz to 3 GHz

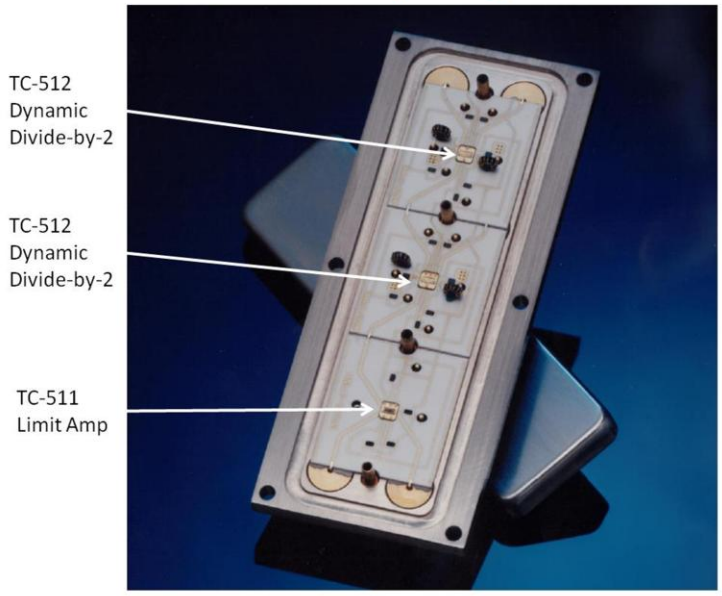
DC-4.5GHz, 18dB Gain, 0.5W Power Amplifier



>This Power Amp designed by Tim Shirley was one of the most profitable of the circuits built with the RFIC process
>At one point it was enabling instrument shipments of over $1M per day!

TC-525
Description: DC-4.5 GHz 0.5 Watt Power Amplifier, 18dB Gain
Designer: T. Shirley
Year Designed:1988
Year Shipped: 8/1990
Shipped in [instrument]: Many – Every DC-4 low-band produced by Hewlett-Packard until the late 90's

HP8665 3GHz – 6GHz Frequency Divider Module



>HP's lowest phase noise signal generator in 1989 used Dynamic frequency dividers designed by Doug Snook to stabilize the YIG oscillator in a Phase locked loop

>Three GaAs ICs were used

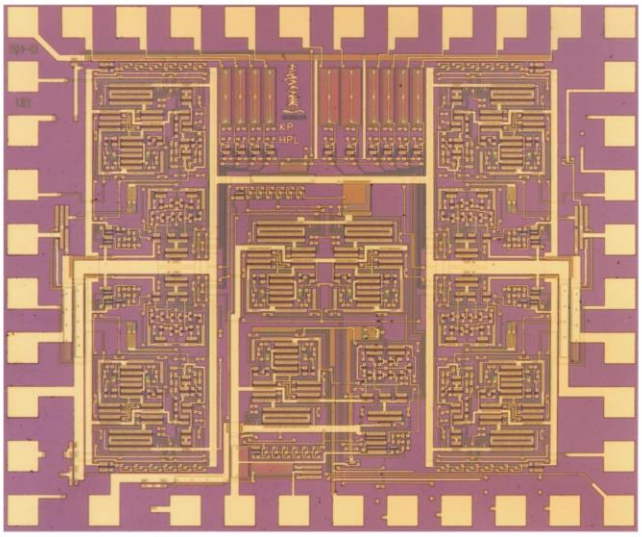
Shipped 1989

Doug Snook, designer

See:

J. Summers and D. Snook, "High-Spectral-Purity Frequency Synthesis in a Microwave Signal Generator," in *HP Journal* Oct., 1989, pg. 37-41.

1 Gsa/sec Track & Hold / 4x Analog Demux



~100 FETs; Thin Film Capacitors a key element; Oscilloscope Front-end

>And finally…

>This 1Gsa/s Track and Hold circuit by Ken Poulton was the most daring design of the period

> It suppressed the slow tail problem with clever circuit design

>A companion GaAs IC digital logic chip controlled the sequence of events

>This circuit became the first in a long line of high-speed track and hold front ends for HP digitizing oscilloscopes

>It first shipped in 1986

>And for a year or two, this circuit enabled the highest sample rate scope in existence, with the highest dollar volume of any single instrument in HP.

TC-506

Description: single T/H circuit at 1 GSa/s, fanning out to 4 T/H's at 250 MHz

Designer: K. Poulton

Year Designed: 1982-85

Year Shipped: 1986

Shipped in [instrument]: 54111D 1 Gsa/s Digital Oscilloscope (and later, the 54112 2 Gsa/s scope)

Conclusion

Starting from Scratch in 1972, we Demonstrated both Digital and RF GaAs ICs Operating to multi-GHz Frequencies

By the Late 1980s, GaAs Monolithic ICs were Firmly Established as High-Performance Components in HP Instruments and Were Commercially Available throughout the Industry.

The HP RFIC Process was in Production for over 20 Years

It Became the Foundation for Subsequent HP IC Processes in GaAs and InP Material Systems: MMICs; p-HEMT MMICs; HBT Digital and Analog ICs

So –

>Starting from Scratch in 1972, we Demonstrated both Digital and RF GaAs ICs Operating to multi-GHz Frequencies

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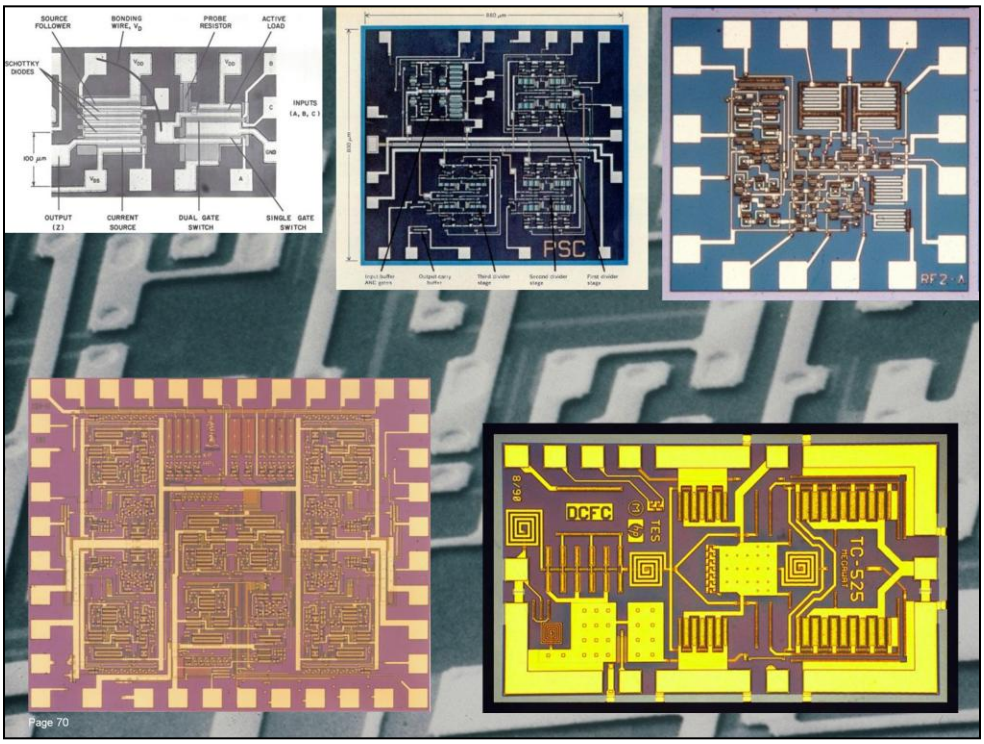

>So here we are, all out of breath for having compressed over one hundred years into 30 minutes

>I hope you have found this bit of history interesting

>And I hope you realize that each of you here has, is, or will be creating Compound Semiconductor IC History of your own.

>Good luck to you!